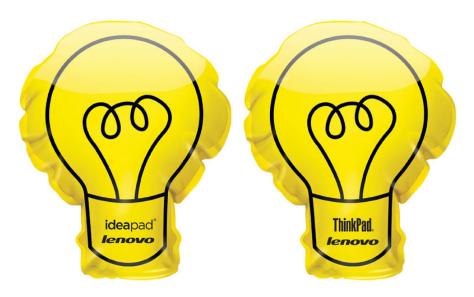
ThinkPad_® ThinkCentre_®

Personal Systems Reference Intel PC Processors - withdrawn

December 2008 - Version 349



lenovo.com

PC Processors (486 family)

	80486SX	80486SX2	80486SL	80486DX	80486DX2
Vendor Code name Type Avail date MHz	P23 CISC Available now 16, 20, 25, 33MHz	Intel CISC Available April 94 50/25MHz	Intel H4C CISC Available now 25, 33MHz	Intel P4 CISC Available now 25, 33, 50MHz	Intel P24 CISC Available now 66/33,50/25,40/20MHz
iCOMP Data bus Processor Address bus Cache	100 at 25MHz 32-bit Data Path 32-bit Processor 32-bit Address Path 8KB unified cache Write-thru 4 way set	180 at 50/25MHz 32-bit Data Path 32-bit Processor 32-bit Address Path 8KB unified cache Write-thru 4 way set	166 at 33MHz 32-bit Data Path 32-bit Processor 32-bit Address Path 8KB unified cache Write-thru 4 way set	249 at 50MHz 32-bit Data Path 32-bit Processor 32-bit Address Path 8KB unified cache Write-thru 4 way set	297 at 66/33MHz 32-bit Data Path 32-bit Processor 32-bit Address Path 8KB unified cache Write-thru 4 way set
Features Voltage	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) * 168 pin / 1.0u 5.0 or 3.3 volts	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 0.8u 5.0 volts	Math cop optional (ThinkPad 350 have none: ThinkPad 750 has one) Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 1.0u 3.3 volts	Math coprocessor std Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 1.0u 5.0 volts	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 0.8u 5.0 volts
OverDrive upgrade	① 486SX2 ② 486DX2 ③ IntelDX4 ④ P24T (Pentium)	① 486DX2 ② IntelDX4 ③ P24T (Pentium)	None	① 486SX2 ② 486DX2 ③ IntelDX4 ④ P24T (Pentium)	① IntelDX4 ② P24T (Pentium)

	IntelDX4 TM	IntelDX4
Vendor Code name Type Avail date	Intel P24C CISC Available April 94	Intel P24D CISC 4th quarter 1995
/ wan date	Available April 04	Hirquartor 1000
MHz iCOMP Data bus Processor Address bus Cache	02 211 2 414 1 411 1	32-bit Data Path 32-bit Processor 32-bit Address Path 16KB unified cache Write-back 4 way set
Features	Math coprocessor std	Math coprocessor std
Voltage	Optimized instructions Address pipelining Burst mode bus (to 160MB/sec) Power mgmt (SMM) 168 pin / 0.6u 3.3 volts	Optimized instructions Address pipelining Burst mode bus (to 160MB/sec) Power mgmt (SMM) 168 pin / 0.6u 3.3 volts
OverDrive upgrade	235/237 pin P24CT based on Pentium technology; 100/50 and 100/33MHz; Available 1996	235/237 pin P24CT based on Pentium technology; 100/50 and 100/33MHz; Available 1996

* Effective June 1993, the 486SX, 486DX, and 486DX2 (called 'SL Enhanced Intel 486^{TM} microprocessors') includes the **486SL** power mgmt technology called System Management Mode (SMM).

Intel OverDrive™ Processor: with a single chip upgrade, gives up to a 70% performance boost w/o modifying external system clock or memory subsystem. The chip may be placed in an open socket on planar or in the socket after the existing processor is removed.

Burst mode bus: for reads and writes from processor to memory; 4 back-to-back data transfers (usually in 5 cycles); 486 is 128-bits (16 bytes) and Pentium CPU is 256-bits (64-bits x 4; (32 bytes).

Mobile Intel®Celeron® Pr	rocessor	
Vendor Positioning Instruction architecture MMX™ / Streaming SIMD	Intel® Value mobile PC IA-32 / P6 microarchitecture / CISC/RISC/micro-ops Yes / 57 new instructions / eight 64-bit MMX registers	Same Same Same MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - size L1 cache - write policy L1 cache - organization L1 cache - bus L1 cache - parity	16KB data; 16KB instruction Write-back or thru (data); write-thru (instruction) 4 way set associative (data); 2 way set associative (instruction) 64-bit / full speed / non-blocking Parity in cache and internal registers	Same Same Same Same Same
L2 cache - size L2 cache - write policy L2 cache - organization L2 cache - bus	128KB (integrated on the die) Write-through or write-back (programmable per line), uncacheable, write-protect 4 way set associative / non-blocking Full speed / 64-bit path / ECC	Same Same Same Same Same Same
System bus - parity System bus - speed System bus - features Bus architecture	ECC on system bus; parity on address bus (frontside) 66MHz Frontside Bus Nonblocking cache hierarchy Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture	Same 100MHz Frontside Bus Same Same Same
Execution units Pipeline stages Supscal dispatch/execute Superscalar issue Superscalar retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating pt unit; 1 load unit; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) / 512 entry BTB Yes Pipelined math coprocessor	Same Same Same Same Same Same Same Same
Internal processing External data bus External address bus User registers Cache line size Power management Multiple processors	32-bits (300 bit internal bus width) / 32-bit word size 64-bit system bus with ECC 36-bits (64GB physical address space; 64TB virtual) 8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) System Management Mode (SMM) No SMP support	Same Same Same Same Same Same Same Same
Technology (micron) CPU voltage	0.25u 1.6 volts (2.5 volts I/O); 1.5 volts (2.5 volts I/O) for 266MHz low voltage;	0.18u 1.6 volts (2.5 volts I/O); 1.35 volts (2.5 volts I/O) for Low Voltage processors;
Power	Supports QuickStart allowing 0.4 watt idle power state	1.1 volts for 500MHz Ultra Low Voltage processors Supports QuickStart allowing 0.4 watt idle power state
Transistors Package type	~18 million 280-pin Mobile Module (MMC1) 400-pin Mobile Module (MMC2) 240-pin Mini-cartridge Ball Grid Array (BGA) Micro Pin Grid Array (Micro-PGA)	~18 million 280-pin Mobile Module (MMC1) 400-pin Mobile Module (MMC2) 240-pin Mini-cartridge Ball Grid Array (BGA) Micro Ball Grid Array (Micro-BGA2) Micro Bin Grid Array (Micro-BGA2)
Frequency (available)	266/66MHz (low voltage) (April 1999) 266/66MHz (January 1999) 300/66MHz (January 1999) 333/66MHz (April 1999) 366/66MHz (May 1999) 400/66MHz (June 1999) 433/66MHz (Sept 1999) 466/66MHz (Sept 1999)	Micro Pin Grid Array (Micro-PGA or Micro-PGA2) 400A/100MHz Low Voltage (February 2000) 450/100MHz (February 2000) 500/100MHz (February 2000) 500/100MHz Ultra Low Voltage (January 2001) 550/100MHz (April 2000) 500/100MHz Low Voltage (June 2000) 600/100MHz (June 2000) 600/100MHz Ultra Low Voltage 1.1v (May 2001) 600/100MHz Low Voltage 1.35v (May 2001) 650/100MHz (June 2000) 700/100MHz (September 2000) 750/100MHz (March 2001) 800/100MHz (July 2001)
Chipset support	440DX, 440BX, 440MX, 440ZX, 440ZX-66	900/100MHz (October 2001) 440DX, 440BX, 440MX, 440ZX, 440ZX-66, 815EM

Mobile Intel® Celeron® P	rocessor	
Vendor Positioning Instruction architecture MMX™ / Streaming SIMD	Intel® Value mobile PC IA-32 / P6 microarchitecture / CISC/RISC/micro-ops MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)	Same Same Same MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - size L1 cache - write policy L1 cache - organization L1 cache - bus L1 cache - parity	16KB data; 16KB instruction Write-back or thru (data); write-thru (instruction) 4-way set associative 64-bit / full speed / non-blocking Parity in cache and internal registers	Same Same Same Same Same Same
L2 cache - size L2 cache - data path L2 cache - buffering	128KB / full speed 64-bit data path / ECC	256KB / full speed (Advanced Transfer Cache) 256-bit data path / quad-wide cache line / ECC Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus que
L2 cache - organization L2 cache - controller L2 cache - write policy L2 cache - type	8-way set associative / non-blocking Integrated / unified (internal die; on die) Write-through or write-back (programmable per line), uncacheable, write-protect	8-way set associative Integrated / unified (internal die; on die) Write-through or write-back (programmable per line), uncacheable, write-protect Non-blocking / pipelined burst synchronous
System bus - parity System bus - speed System bus - features Bus architecture	ECC on system bus; parity on address bus (frontside) 133MHz frontside bus Nonblocking cache hierarchy Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture	Same 100MHz or 133MHz frontside bus Same Same Same Same
Execution units Pipeline stages Supscal dispatch/execute Superscalar issue Superscalar retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating pt unit; 1 load unit; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) / 512 entry BTB Yes Pipelined math coprocessor	Same Same Same Same Same Same Same Same
Internal processing External data bus External address bus User registers Cache line size Power management Multiple processors	32-bits (300 bit internal bus width) / 32-bit word size 64-bit system bus with ECC 36-bits (64GB physical address space; 64TB virtual) 8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) Quick Start and Deep Sleep No SMP support	Same Same Same Same Same Same Same Same
Technology (micron) CPU voltage Package type	0.18u 1.7 volts Micro-Flip Chip Ball Grid Array (Micro-FCBGA)	1.1 volts for Ultra Low Voltage processors 1.15 volts for Low Voltage processors 1.4 or 1.45 volts for others Micro-Flip Chip Ball Grid Array (Micro-FCBGA)
Frequency (available)	Micro-Flip Chip Pin Grid Array (Micro-FCPGA) 733MHz (October 2001) 800A MHz (October 2001) 866MHz (October 2001) 933MHz (October 2001)	Micro-Flip Chip Pin Grid Array (Micro-FCPGA) 650/100MHz Ultra Low Voltage (January 2002) 650/100MHz Low Voltage (October 2001) 700MHz/100MHz Ultra Low Voltage (September 2002) 733MHz/133MHz Low Voltage (April 2002)
	The "A" is added to the "800A" in Micro-FCBGA and Micro-FCPGA to distinguish it from the Mobile Intel Celeron Processor 800MHz in Micro-BGA2 and Micro-PGA2 packages	733MHz/133MHz Ultra Low Voltage (September 2002) 800MHz/133MHz Ultra Low Voltage (January 2003) 866MHz/133MHz Low Voltage (January 2003) 1GHz/133MHz (April 2002) 1.06GHz/133MHz (January 2002) 1.13GHz/133MHz (January 2002) 1.2GHz/133MHz (January 2002) 1.33GHz/133MHz (June 2002)

Mobile Intel® Celeron® for value mobile systems					
Code name Micro-architecture MMX TM / Streaming SIMD SSE2 Power mgmt technology	Northwood IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) AutoHALT, Stop-Grant, Sleep, Deep Sleep				
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)				
L2 cache - size L2 cache - data path	256KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC				
System bus Memory addressability System bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path				
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit				
Out-of-order instructions Branch prediction Speculative execution Math coprocessor	Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers				
Compatibility Multiple processors	Compatible with IA-32 software No SMP support				
Technology (micron) Voltage Package and connector	0.13u 1.3 volts Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket				
Frequency (MHz) and available date	1.26GHz available April 2003 1.4GHz available June 2002 1.5GHz available June 2002 1.6GHz available September 2002 1.7GHz available September 2002 1.8GHz available September 2002 2.0GHz available September 2002 2.0GHz available January 2003 2.2GHz available April 2003 2.4GHz available June 2003 2.5GHz available November 2003				
Chipset support	Intel 845MZ with DDR-SDRAM memory Intel 845MP with DDR-SDRAM memory Intel 852GM, 852GME, 852PM with DDR-SDRAM memory Other compatible chipsets				

Intel® Celeron® M proces	ssor for mobile systems						
Code name Messaging	Banias Celeron or ICP-M Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs						
Micro-architecture MMX™ / Streaming SIMD SSE2	1A-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus 0 MMX™ (57 new instructions) / Streaming SIMD Extensions 2 (144 new instructions)						
	Auto Halt, Stop Grant, Deep S						
L1 cache - bus	256-bit data path / full speed						
L1 data cache	32KB data cache / integrated						
L1 instruction cache	32KB instruction cache / integ	grated					
L2 cache - size	512KB / full speed (Advanced			. A constitutive / into supplied / varified / into supplied in the distance of the latest supplied in the supp			
L2 cache - data path L3 cache	None	64 byte cache iir	ne size / 8-way se	et associative / integrated / unified (internal die; on die)			
System bus Memory addressability	400MHz (transfers data four t			sfers at two times per clock / 64 byte cache line size			
System bus - width	64-bit data path	7 00 bit addressi	ing / address bas	15 double clocked at 250Wi iz			
Execution units	2 integer units; 1 floating poin	t units; 1 load un	it; 1 store unit				
	Yes (out-of-order instruction e						
Branch prediction Speculative execution	Dynamic (based on history) Yes (Advanced Dynamic Exec	sution)					
Math coprocessor	Pipelined floating point unit	oution)					
Compatibility	Compatible with IA-32 softwa	re					
Multiple processors	No SMP support						
Technology (micron) Package and connector	0.13u Micro Flip-Chip Pin Grid Arı	ray (Micro-FCP0	GA) requires 479	-pin surface mount Zero Insertion Force (ZIF) sock			
•	(mPGA479M socket) or Mic	ro Flip-Chip Bal	II Grid Array (Mi	cro-FCBGA) for surface mount (479-ball)			
		Voltage Th	nermal Design Po				
Frequency (MHz/GHz)	800MHz Ultra Low Voltage	1.004 volts	7 watts	<i>date</i> January 2004			
and available date	900MHz Ultra Low Voltage	1.004 volts	7 watts	April 2004			
	1.2GHz	1.356 volts	24.5 watts	January 2004			
	1.3GHz	1.356 volts	24.5 watts	January 2004			
	1.4GHz	1.356 volts	24.5 watts	April 2004			
Chipset support	Intel 855 chipset family Intel 852GM						
	Other compatible chipsets						

Intel® Celeron® M process	sor for mobile system.	S Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Available date
Intel Celeron M Processor	Ultra Low Voltage 353	900MHz	512KB	No	400MHz	No	July 2004
Intel Celeron M Processor		1.0GHz	512KB	Yes	400MHz	No	January 2005
Intel Celeron M Processor		1.0GHz	1MB	Yes	400MHz	No	April 2005
	-						
ntel Celeron M Processor		1.2GHz	512KB	No	400MHz	No	January 2004
ntel Celeron M Processor		1.3GHz	512KB	No	400MHz	No	January 2004
ntel Celeron M Processor	330	1.4GHz	512KB	No	400MHz	No	April 2004
ntel Celeron M Processor	340	1.5GHz	512KB	No	400MHz	No	June 2004
ntel Celeron M Processor	350	1.3GHz	1MB	No	400MHz	No	August 2004
ntel Celeron M Processor	350J	1.3GHz	1MB	Yes	400MHz	No	August 2004
ntel Celeron M Processor		1.4GHz	1MB	No	400MHz	No	August 2004
ntel Celeron M Processor	360.1	1.4GHz	1MB	Yes	400MHz	No	August 2004
ntel Celeron M Processor		1.5GHz	1MB	Yes	400MHz	No	January 2005
Intel Celeron M Processor		1.6GHz	1MB	Yes	400MHz	No	July 2005
Intel Celeron M Processor		1.7GHz	1MB	Yes	400MHz	No	January 2005
THE OCICION WIT TOCC3301		1.7 0112		103	400WII 12	110	January 2000
Messaging Micro-architecture MMX™ / Streaming SIMD SSE2 SSE3 Hyper-Threading Power mgmt technology	level of mobile processon IA-32 / micro-op fusion,	re designed sor technology dedicated strictions) / Strear sions 2 (144 r	and excep ack manag ming SIMD new instruction	otional value in er, advanced Extensions (* ep	n sleeker, light branch predic 70 new instruc	er notebook desigr tion, power-optimiz	cessor delivers a balanc ns zed processor system b
_1 cache - bus	256-bit data path / full s	need					
	32KB data cache / integ						
	32KB data cache / Integ 32KB instruction cache	•					
LT INSTRUCTION CACHE	32ND IIISII UCIIOII CACHE	/ integrated					
L2 cache - data path	512KB or 1MB / full spe 256-bit data path (32 by None				set associativ	e / integrated / unif	fied (internal die; on die)
Memory addressability	400MHz (transfers data 64GB memory address 64-bit data path						64 byte cache line size
Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floatin Yes (out-of-order instruct Dynamic (based on hist Yes (Advanced Dynami Pipelined floating point Compatible with IA-32 s	ction execution cory) c Execution) unit		; 1 store unit			
Package and connector	310 to 340: 130nm (nar Micro Flip-Chip Pin Gi (mPGA479M socket) c	id Array (Mi	cro-FCPG	A) requires 4	79-pin surfac	e mount Zero Ins	ertion Force (ZIF) sock int (479-ball)
_				U	Thermal De	0	
' '	353: 900MHz Ult r	•	•	0.0940 vo			
	373/383: 1.0GHz Ultra	a Low Voltag	е	0.0940 vo	lts 5 wa	tts	
	310: 1.2GHz			1.356 volt	s 24.5	watts	
	320: 1.3GHz			1.356 volt	s 24.5	watts	
	330: 1.4GHz			1.356 volt		watts	
	340: 1.5GHz			1.356 volt	-	watts	
	350/350J: 1.3GHz			1.260 volt			
	360/360J: 1.4GHz			1.260 volt			
	370: 1.5GHz			1.260 volt			
	380: 1.6GHz 390: 1.7GHz			1.260 volt 1.260 volt			
Chipset support	Intel 852GM chipset Intel 855 chipset famil	v		200 4011	. Li W		
	Mobile Intel 910GML E	•	set				
				mily			
	Mobile Intel 915 and 9	•	Cilipset fai	шиу			
	Other compatible chip	sets					

[Mobile] Intel Celeron M Processor 4xx

Intel® Celeron® M processor for mobile systems	Clock Speed	L2 cache	System bus MHz		Hyper- Threading Fechnology	threads	ization		Enhanced Intel SpeedStep™ Technology	Intel 64 Tech		Avail- able date
Intel Celeron M Processor Ultra Low Voltage 423	1.06GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Apr	2006
Intel Celeron M Processor Ultra Low Voltage 443	1.20GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Jan	2007
Intel Celeron M Processor 410	1.46GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	May	2006
Intel Celeron M Processor 420	1.60GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Apr	2006
Intel Celeron M Processor 430	1.73GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Apr	2006
Intel Celeron M Processor 440	1.86GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Sep	2006
Intel Celeron M Processor 450	2.00GHz	1MB	533MHz	Single	e No	1	No	Yes	No	No	Sep	2006

Processor generation Yonah

Marketing name Intel Celeron M Processor

Core Single-core

Centrino[™] Not part of the Centrino branding

Micro-architecture IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus

MMX™ / Streaming SIMD MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)

SSE2 Streaming SIMD Extensions 2 (144 new instructions)
SSE3 Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology Auto Halt, Stop Grant, Deep Sleep low power C-states

Thermal management Thermal management system (digital temperature sensor and thermal monitor)

Hyper-Threading None

Total threads One thread (one cores with no Hyper-Threading support provides one logical processor)

Execute Disable (XD) Bit Protects memory data areas from malicious software execution

Intel 64 Technology¹ None Virtualization Technology None

L1 cache - bus 256-bit data path, full speed
L1 data cache 32KB data cache / integrated
L1 instruction cache 32KB instruction cache / integrated

L2 cache - size 1MB / full speed / Advanced Transfer Cache / Data Cache Unit Streamer

L2 cache - data path 256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)

L3 cache None

System bus - width

System bus 533MHz (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size

Memory addressability 64GB memory addressability / 36-bit addressing / address bus is double clocked at 266MHz

64-bit data path

Execution units 2 integer units, 1 floating point units, 1 load unit, 1 store unit

Math coprocessor Pipelined floating point unit Compatibility Compatible with IA-32 software

Process technology 65nm or 0.065u

Power Ultra Low Voltage: 5.5 watts; 420/430: 27 watts

Package and connector Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket

(mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)

[Ultra Low Voltage offered only in Micro Flip-Chip Ball Grid Array (Micro-FCBGA)]

Chipset support Mobile Intel 945 Express Chipset family,
Mobile Intel 940GML Express Chipset,

other compatible chipsets

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(M4INTEL) Compiled by Roger Dodson, Lenovo. December 2007

Celeron®			
Code name Vendor Positioning Instruction architecture MMX technology Streaming SIMD	Covington Intel® Value PC desktops IA-32 / P6 microarchitecture / CISC/RISC/micro-ops Yes / 57 new instructions / eight 64-bit MMX registers None	Mendocino Same Same Same Same Same 566MHz and higher:	Celeron® is based on the same P6 core architecture as the Pentium II : Streaming SIMD Extensions
L1 cache - controller L1 cache - size L1 cache - write policy L1 cache - organization L1 cache - bus L1 cache - type; parity	Integrated 16KB data; 16KB instruction Write-back or thru (data); write-thru (instruction) 4-way set associative (data); 2-way set associative (instructn) 64-bit / full speed Non-blocking; parity in cache and internal registers	Same Same Same Same Same Same	
L2 cache - controller L2 cache - size L2 cache - write policy L2 cache - organization L2 cache - bus	None None N/A N/A None	Integrated 128KB (integrated of Write-through or write uncacheable, 4 way set associative) Full speed / ECC	te-back (programmable per line), write-protect
System bus - parity System bus - speed System bus - features Bus architecture	ECC on system bus; parity on address bus (frontside) 66MHz Nonblocking cache hierarchy 8 entry transactional buffer for system bus Frontside bus only since no L2 cache (backside bus) / no Dual Independent Bus Architecture (DIB)	Same 66MHz or 100MHz Same Same Independent backsid	de and frontside buses operate ndependent Bus Architecture
Execution units Pipeline stages Supscaldispatch/execute Superscalar issue Superscalar retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating point unit; 1 load; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) Yes Pipelined math coprocessor	Same as having Same does not it Same Same The "A" is Same as having	s added to the "300A" to distinguish it g L2 cache as the "300"MHz version have L2 cache s added to the "533A" to distinguish it g FC-PGA packaging as the z version uses SEP packaging
Internal processing External data bus External address bus User registers Cache line size Multiple processors	32-bits (300 bit internal bus width); 32-bit word size 64-bit system bus with ECC 36-bits (64GB physical address space; 64TB virtual) 8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) / Addr-data-data-data-data No SMP support	Same Same Same Same Same Same	
Technology Die area CPU voltage Transistors Package type	0.25u CMOS 139.9 sq mm 2.0 volt core ~7.5 million Single Edge Processor (SEP) package requires Intel Slot 1	433MHz) - Plastic Pin Grid A (300A, 333, 366, 4 - Flip-Chip Pin Gri	,
Available date Frequency	May 1998 266MHz, 300MHz / 66MHz system bus	900, 950MHz, 1G August 1998 (300A March 1999 (433); A January 2000 (533); June 2000 (633, 677 January 2001 (800); August 2001 (950, 1 300AMHz, 333MHz 466MHz, 500MHz, 5	Hz, 1.10 GHz) and 366); Jan 1999 (366 and 400) April 1999 (466); August 99 (500); ; March 2000 (566 and 600); 7, 700); November 2000 (733, 766); ; April 2001 (850); July 2001 (900); IGHz, 1.10GHz) , 366MHz, 400MHz, 433MHz, 533MHz, 533A, 566MHz,
Chipset support	440EX is preferred (does support 440LX, 440BX) sperty of their respective owners	766 , 800, 850, 900, Frontside bus 440ZX-66, 810, 810 preferred (does su	667MHz, 700MHz, all have 66MHz Frontside bus .950MHz, 1GHz, 1.10 GHz / 100MHz E, 810E2, 815, 815E, 815EP is pport 440EX, 440LX, or 440BX)

Celeron®	
Code name Vendor Positioning Instruction architecture MMX technology Streaming SIMD	Tualatin Intel® Value PC desktops IA-32 / P6 microarchitecture / CISC/RISC/micro-ops Yes / 57 new instructions / eight 64-bit MMX registers Streaming SIMD Extensions
L1 cache - controller L1 cache - size L1 cache - write policy L1 cache - organization L1 cache - bus L1 cache - type; parity	Integrated 16KB data; 16KB instruction Write-back or thru (data); write-thru (instruction) 4-way set associative (data); 2-way set associative (instruction) 64-bit / full speed Non-blocking; parity in cache and internal registers
L2 cache - size L2 cache - data path L2 cache - buffering L2 cache - organization L2 cache - controller L2 cache - write policy L2 cache - type	256KB / full speed (Advanced Transfer Cache) 256-bit data path / quad-wide cache line / ECC Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) 8-way set associative Integrated / unified (internal die; on die) Write-through or write-back (programmable per line), uncacheable, write-protect Non-blocking / pipelined burst synchronous
System bus - parity System bus - speed System bus - features Bus architecture	ECC on system bus; parity on address bus (frontside) 100MHz Frontside Bus Nonblocking cache hierarchy 8 entry transactional buffer for system bus Independent backside and frontside buses operate concurrently / Dual Independent Bus architecture
Superscalar issue Superscalar retire	2 integer/MMX units; 1 floating point unit; 1 load; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) Yes Pipelined math coprocessor
Internal processing External data bus External address bus User registers Cache line size Multiple processors	32-bits (300 bit internal bus width); 32-bit word size 64-bit system bus with ECC 36-bits (64GB physical address space; 64TB virtual) 8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) / Addr-data-data-data No SMP support
Technology Package type	0.13u process technology Flip-Chip Pin Grid Array 2 (FC-PGA2) for 370-pin zero insertion force socket (PGA370 socket)
Available date	October 2001 (1.20GHz) January 2002 (1.30GHz) June 2002 (1.40GHz)
Frequency	1.20 GHz / 100MHz Frontside bus 1.30 GHz / 100MHz Frontside bus 1.40 GHz / 100MHz Frontside bus
Chipsetsupport	Intel 440BX, 440ZX, 810 series, 815, series, and others

Intel® Celeron® for value	desktop systems
Code name Micro-architecture MMX™/Streaming SIMD SSE2	Willamette IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path	128KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Frontside bus Memory addressability Frontside bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Cache line size Multiple processors	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data No SMP support
Technology (micron) Transistors Package and connector	0.18u ~42 million with die size of 217 square millimeters Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)
Frequency (MHz) and available date	1.7GHz available May 2002 1.8GHz available June 2002
Chipsetsupport	Intel 845 family

Intel® Celeron® for value	Intel® Celeron® for value desktop (and mobile) systems					
Code name Micro-architecture MMX™ / Streaming SIMD SSE2	Celeron Northwood IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)					
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)					
L2 cache - size L2 cache - data path	128KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC					
Frontside bus Memory addressability Frontside bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path					
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers					
Compatibility Multiple processors	Compatible with IA-32 software No SMP support					
Technology (micron) Package and connector	0.13u Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)					
Frequency (MHz) and available date	2.0GHz available September 2002 2.1GHz available November 2002 2.2GHz available November 2002 2.2GHz available June 2003 for mobile systems 2.3GHz available March 2003 2.3GHz available June 2003 for mobile systems 2.4GHz available June 2003 for mobile systems 2.4GHz available June 2003 for mobile systems 2.5GHz available June 2003 for mobile systems 2.5GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.6GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.7GHz available September 2003 for both desktop and mobile systems (transportable processors) 2.8GHz available November 2003 for both desktop and mobile systems (transportable processors)					
Chipsetsupport	Intel 845 and 865 desktop family and others Intel 852GM, 852GME, 852PM mobile chipset					

[Desktop] Intel Celeron D Processor 3xx

Intel® Celeron® D Proces	sor for des	sktop s	ystems				Faharra	lm4-1		
		Clock speed	L2 cache	System bus	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Process	Available date
Intel Celeron D Processo	r 320 2.	40GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processo			256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processo	r 325J 2.	53GHz	256KB	533MHz	Yes	No	No	No	90nm	June 2004
Intel Celeron D Processo	r 326 2.	53GHz	256KB	533MHz	Yes	No	No	Yes	90nm	May 2005
Intel Celeron D Processo	r 330 2.0	66GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processo	r 330J 2.0	66GHz	256KB	533MHz	Yes	No	No	No	90nm	June 2004
Intel Celeron D Processo		66GHz	256KB	533MHz	Yes	No	No	Yes	90nm	May 2005
Intel Celeron D Processo	r 335 2.8	80GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processo	r 335J 2.8	80GHz	256KB	533MHz	Yes	No	No	No	90nm	June 2004
Intel Celeron D Processo	r 336 2.8	80GHz	256KB	533MHz	Yes	No	No	Yes	90nm	May 2005
Intel Celeron D Processo	r 340 2.9	93GHz	256KB	533MHz	No	No	No	No	90nm	September 2004
Intel Celeron D Processo	r 340J 2.9	93GHz	256KB	533MHz	Yes	No	No	No	90nm	September 2004
Intel Celeron D Processo			256KB	533MHz	Yes	No	No	Yes	90nm	May 2005
Intel Celeron D Processo			256KB	533MHz	No	No	No	No	90nm	November 2004
Intel Celeron D Processo			256KB	533MHz	Yes	No	No	No	90nm	November 2004
Intel Celeron D Processo				533MHz	Yes	No	No	Yes	90nm	May 2005
										•
Intel Celeron D Processo				533MHz	Yes	No	No	Yes	65nm	October 2006
Intel Celeron D Processo			256KB		Yes	No	No	No	90nm	June 2005
Intel Celeron D Processo			256KB		Yes	No	No	Yes	90nm	June 2005
Intel Celeron D Processo				533MHz	Yes	No	No	Yes	65nm	May 2006
Intel Celeron D Processo	r 355 3.	33GHz	256KB	533MHz	Yes	No	No	Yes	90nm	December 2005
Intel Celeron D Processo	r 356 3.	33GHz	512KB	533MHz	Yes	No	No	Yes	65nm	May 2006
Intel Celeron D Processo	r 360 3.4	46GHz	512KB	533MHz	Yes	No	No	Yes	65nm	Sept 2006
Intel Celeron D Processo	r 365 3.0	60GHz	512KB	533MHz	Yes	No	No	Yes	65nm	January 2007
Processor generation	Prescott (′90nm) c	or Codar	Mill (65nn	n)					
Core	,	,		`	ium 4) core					
	-			,	,		nar ninalinad ta	مامعطم	~	
Micro-architecture						tage pipeline (Hy		CHHOIO	gy)	
MMX™ / Streaming SIMD							ew instructions)			
SSE2				,	new instruct	,				
SSE3	Streaming	SIMDE	Extension	ıs 3 (13 ne	w instruction	ons)				
Hyper-Threading	No									
Execute Disable Bit	Some: pro	otects m	emory da	ata areas t	from malicion	ous software exec	cution			
Intel 64 Technology ¹	Some: Inte	el 64 Te	chnology	•						
L1 cache - bus	256-bit data path / full speed									
L1 data cache	16KB data	cache /	/ 4-way s	et associa	tive / write-	through / 64 byte	cache line / inte	egrated		
L1 instruction cache						way set associativ				
	called Exe	cution T	race Cac	he; cache	s decoded :	x86 instructions (i	micro-ops)			
L2 cache - size	256KB or	512KB	/ full spec	ed (Advan	ced Transfe	r Cache)				
L2 cache - data path				•		ous clock / 128 by	te cache line si	ze (usu	ally divided	into two 64 byte
22 dadilo data patil				•		fied (internal die;		20 (404	any arriada	into the or byto
L3 cache	None	o-way se	et associ	alive / lille	grateu / urii	neu (internaruie,	on die) / LCC			
L3 cache	None									
System bus	522MU- /+	tranefore	data for	ır timos no	r clock) / ac	ddress bus transfe	ore at two times	nor de	ock /	
System bus	`			ii iiiiles pe	i clock) / ac	Juless bus transit	ers at two times	per cio	CK /	
	64 byte ca					,				
Memory addressability		• .	dressabil	ity / 36-bit	addressing	/ address bus is	double clocked	at 200,	266, or 40	OMHZ
System bus - width	64-bit data	a path								
Execution units	2 integer u	ınits; 1 fl	loating po	oint units;	1 load unit;	1 store unit				
	Two intege	er units (or Arithm	netic Logic	Units) run	at two times core	frequency (Rai	pid Exe	cution Engi	ne)
Out-of-order instructions	Yes	`		9 -	,		. , , ,		3	•
		based o	n history) / 4KB Br	anch Target	Buffer				
Branch prediction			•	,	anon rargo	Danoi				
	Vac (Advai			,	129 bit floo	ting point registe	re			
Speculative execution	Yes (Advar	,	naint unit		120-011 1106	illig politi registe	10			
Speculative execution	Yes (Advar Pipelined f	,	point unit	. / Hariules						
Speculative execution Math coprocessor	Pipelined f	floating				La with EMCAT as	fta.ua\			
Speculative execution Math coprocessor Compatibility	Pipelined f	floating e with IA	\-32 soft\	ware (som		le with EM64T so		l		
Speculative execution Math coprocessor	Pipelined f	floating e with IA	\-32 soft\	ware (som		le with EM64T so .1 standard test a		bounda	ary scan	
Speculative execution Math coprocessor Compatibility	Pipelined f Compatible Thermal m	floating e with IA nonitorin	\-32 soft\ g, built-ir	ware (som n self test,	IEEE 1149	.1 standard test a	ccess port and			
Speculative execution Math coprocessor Compatibility Other features Process technology	Pipelined f Compatible Thermal m Prescott: 9	floating e with IA nonitorin 90nm (n	A-32 softvig, built-ir	ware (som n self test, r) or 0.09u	IEEE 1149	.1 standard test a Cedar Mill: 65nm	(nanometer) or	0.065u	(micron)	
Speculative execution Math coprocessor Compatibility Other features Process technology	Pipelined f Compatible Thermal m Prescott: 9	floating e with IA nonitorin 90nm (n	A-32 softvig, built-ir	ware (som n self test, r) or 0.09u	IEEE 1149	.1 standard test a Cedar Mill: 65nm	(nanometer) or	0.065u	(micron)	rtion Force (ZIF)
Speculative execution Math coprocessor Compatibility Other features Process technology	Compatible Thermal m Prescott: S All: Flip-C	floating e with IA nonitorin 90nm (n Chip Pir	A-32 softv ig, built-ir anomete in Grid Ar	ware (som n self test, r) or 0.09u	IEEE 1149 u (micron); (n PGA4) pa	.1 standard test a Cedar Mill: 65nm	(nanometer) or	0.065u	(micron)	rtion Force (ZIF)
Speculative execution Math coprocessor Compatibility Other features Process technology	Compatible Thermal m Prescott: S All: Flip-C socke	e with IA nonitorin 90nm (n Chip Pir	A-32 softvig, built-ir anomete Grid Ar	ware (som n self test, er) or 0.09u rray (FC-n	u (micron); on PGA4) packet	.1 standard test a Cedar Mill: 65nm	(nanometer) or	0.065u moun	(micron) t Zero Inse	
Math coprocessor Compatibility	Compatible Thermal m Prescott: S All: Flip-C socke	e with IA nonitorin 90nm (n Chip Pir	A-32 softwag, built-ir anomete an Grid Ar an mPGA	ware (som n self test, r) or 0.09u ray (FC-n 478B soc 75-land F	u (micron); on PGA4) packet	.1 standard test a Cedar Mill: 65nm ckage requires 4 nd Grid Array (F	(nanometer) or	0.065u moun	(micron) t Zero Inse	, ,
Speculative execution Math coprocessor Compatibility Other features Process technology Package and socket	Pipelined f Compatible Thermal m Prescott: S All: Flip-C socke All except	e with IA nonitorin 90nm (n Chip Pir et name 320 and	A-32 softwag, built-ir anomete of Grid Ared mPGA	ware (som n self test, rr) or 0.09u rray (FC-n 478B soc 75-land Fl socket also	u (micron); (mPGA4) packet lip-Chip La	.1 standard test a Cedar Mill: 65nm ckage requires 4 nd Grid Array (Fisket T)	(nanometer) or 178-pin surface	0.065u e moun	(micron) t Zero Inse	
Speculative execution Math coprocessor Compatibility Other features Process technology	Pipelined f Compatible Thermal m Prescott: \$ All: Flip-C socke All except FC-mPGA	e with IA nonitorin 90nm (n Chip Pir et name 320 and	A-32 softvig, built-ir anomete a Grid Ared mPGA d 350: 7 (s	ware (som n self test, rr) or 0.09u ray (FC-n 478B soc 75-land Fl socket also 845 family	u (micron); (mPGA4) packet lip-Chip Lac o called Soc, 848P, 865	.1 standard test a Cedar Mill: 65nm ckage requires 4 nd Grid Array (F	(nanometer) or 178-pin surface	0.065u e moun	(micron) t Zero Inse	

PC Processors (Pentium)

Cache Soft Cache - write policy Write Cache - organization	el® cong performance; ftware compatibility SC/RISC B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	P54C Same Same Same Same Same Same Same Same	P54LM (120, 133, and 150 MHz is P54CSLM) Same; Mobile systems Same Same Same Same Same Same Same Value (in block) Lower Voltage (2.9 v)	P54CQS Same Same Same Same Same Same Same Sam	P54CS Same Same Same Same Same Same Same Sam
Vendor Intel Positioning Strom Soft Instruction architecture CISC Cache	el® cong performance; ftware compatibility SC/RISC B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same Same Same Same Same	150 MHz is P54CSLM) Same; Mobile systems Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same
Positioning Stroi Softs Instruction architecture CISC Cache Cache - write policy Write Write Cache - organization 2 was Cache - parity Parity Parity Parity 1 Superscalar issue 2 into 2 Superscalar execution 2 into 2 Superscalar execution Dyna Speculative execution Math coprocessor Pipe Internal processing External data bus External address bus Word size User registers 8 GF	ong performance; ftware compatibility SC/RISC B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same Same Same Same Same	Same; Mobile systems Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same
Cache SKB Cache - write policy Write Cache - organization 2 wa Cache - parity Parity Parity Parity Execution units 2 fixe 1 Superscalar issue 2 int 2 Superscalar execution 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF	ftware compatibility SC/RISC B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same Same Same Same Same	Mobile systems Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same
Instruction architecture CISC Cache	B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating point per cycle integers per cycle or 2 floating per cycle integers per cycle or 2 floating per cycle integers per cycle or 2 floatin	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Same
Cache SKB Cache - write policy Write Write Cache - organization 2 wa Cache - parity Parity Parity Execution units 2 fixe 1 Superscalar issue 2 int 2 Superscalar execution 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External address bus Word size 32-b User registers 8 GF	B data; 8KB instruction ite-back or thru (data) ite-thru (instruction) way set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same Same Same Same	Same Same Same Same Same Same Same Voltage (2.9 v)	Same Same Same Same Same Same Of the block o	Same Same Same Same Same Same Same
Cache - write policy Write Write Cache - organization 2 was Cache - parity Pari	rite-back or thru (data) rite-thru (instruction) vay set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same Same	Same Same Same Same Same (in block) Lower voltage (2.9 v)	Same Same Same Same Same (in block) QS means Quick	Same Same Same Same Same
Cache - organization Cache - parity P	rite-thru (instruction) vay set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same Same	Same Same Same Same (in block) Lower voltage (2.9 v)	Same Same Same Same (in block) QS means Quick	Same Same Same
Cache - organization Cache - parity P	rite-thru (instruction) vay set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same	Same Same (in block) Lower voltage (2.9 v)	Same Same (in block) QS means Quick	Same Same Same (in block)
Cache - organization Cache - parity P	vay set associative (both) rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same	Same Same (in block) Lower voltage (2.9 v)	Same Same (in block) QS means Quick	Same Same Same (in block)
Cache - parity P	rity in cache rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same Same	Same Same (in block) Lower voltage (2.9 v)	Same Same (in block) QS means Quick	Same Same Same (in block)
Parity Parity Execution units 2 fixe 1 Superscalar issue 2 int 2 Superscalar execution 2 Superscalar execution 2 Out-of-order instruct No Exanch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus Word size 32-b User registers 8 GF	rity on all external data and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same	Same (in block) Lower voltage (2.9 v)	Same (in block) QS means Quick	Same Same (in block)
Execution units 2 fixe 1 Superscalar issue 2 into 2 Superscalar execution 2 into 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus Word size 32-b User registers 8 GF	and address transfers xed point units and 1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same Same	Same (in block) Lower voltage (2.9 v)	Same (in block) QS means Quick	Same (in block)
Superscalar issue 2 into 2 Superscalar execution 2 into 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF	1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same	Lower voltage (2.9 v)	QS means Quick	` ′
Superscalar issue 2 into 2 Superscalar execution 2 into 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External address bus 44-b External address bus 32-b Word size 32-b User registers 8 GF	1 floating point unit ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)	Same	Lower voltage (2.9 v)	QS means Quick	` ′
Superscalar issue 2 int 2 Superscalar execution 2 int 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus Word size 32-b User registers 8 GF	ntegers per cycle or 2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)		voltage (2.9 v)		
Superscalar execution 2 into 2 Out-of-order instruct Branch prediction Speculative execution Math coprocessor Pipe Internal processing Sexternal data bus External address bus Word size User registers 8 GF	2 floating point per cycle ntegers per cycle or 2 floating point per cycle namic (based on history)				
Superscalar execution 2 into 2 Out-of-order instruct Branch prediction Dyna Speculative execution Math coprocessor Pipe Internal processing 32-b External data bus External address bus Word size 32-b User registers 8 GF	ntegers per cycle or 2 floating point per cycle namic (based on history)	Same			P54CQS but now
Out-of-order instruct Branch prediction Speculative execution Math coprocessor Internal processing External data bus External address bus Word size User registers No Dyna No Pipe 104 No Pipe 105 No	2 floating point per cycle namic (based on history)	Same	Pentium	chip using .35u	also reduced
Out-of-order instruct Branch prediction Speculative execution Math coprocessor Internal processing External data bus External address bus Word size User registers No Dyna Speculative A Speculative Speculative No Pipe Speculat	namic (based on history)		used for mobile	process, but left on	packaging size
Branch prediction Dyna Speculative execution No Math coprocessor Pipe Internal processing External data bus External address bus Word size 32-b User registers 8 GF	namic (based on history)	_	computing (with	P54C packaging size	from P54C/
Speculative execution Math coprocessor Pipe Internal processing S2-b External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF	` ','	Same	no OverDrive).		P54CQS of 253
Math coprocessor Pipe Internal processing 32-b External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF		Same	Uses Voltage		mm to 142 mm
Internal processing 32-b External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF		Same	Reduction		
External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF	pelined math coprocessor	Same	Technology (VRT)		
External data bus 64-b External address bus 32-b Word size 32-b User registers 8 GF	-hits	Same	Same	Same	Same
External address bus 32-b Word size 32-b User registers 8 GF		Same	Same	Same	Same
Word size 32-b User registers 8 GF			Same	Same	Same
User registers 8 GF		Same			
S .		Same	Same	Same	Same
Cache line size 32 b	SPR, 8 FP stack	Same	Same	Same	Same
	,	Same	Same	Same	Same
	dr-data-data-data	Same	Same	Same	Same
,	stem Management Mode (SMM)	Same	Same	Same	Same
	quires external chip	Multiple processor	Same	Same	Same
	set design	ready via built in APIC			
Die area 294	4 sq mm	146 sq mm (original); 228 sq mm (Level C2)	Same	135 sq mm (active) w/ 253 sq mm die	142 sq mm
Technology 0.8u	Bu BiCMOS	0.6u BiCMOS	Same	0.35u BiCMOS	Same
07) volts	3.3 volts	2.9 volts internal	3.3 volts	Same
Cuppiy voltage 0.0 v	, volto	0.0 voits	but 3.3 v external	0.0 voito	Came
Dower (typical/may) 12/1	/16 watts	4/40 wette	4/8 watts	4/10 wotto (120/60)	5.4/14.5 (166/66)
(.)	million	4/10 watts	Same	4/10 watts (120/60)	
	-	Same		Same	Same
Package 273	3 pin grid array	296 pin grid array or	Tape Carrier	296 pin grid array	Same
		TCP for 90/60 and 75/50MHz	Package (TCP)		
Available date June	ne 1993	March 1994	May 1995	March 1995	October 1995
Frequency 60,6	, 66MHz	75/50, 90/60,	75/50, 90/60, 100/66,	120/60, 133/66MHz	133/66, 150/60,
12.2.7	, ···· =	100/66, and	120/60, 133/66 and	,	166/66, and
		120/60MHz	150/60MHz		200/66MHz
OverDrive® upgrade P5T	Tuniprocessor; 273 pin;	P54CT uniprocessor;	None	P54CT for 120/60;	P54CTB
	available 1996	320 pin;	140110	P54CTB for 133/66MHz	(none for 200MHz)
av	avaliable 1990	available 1996		. STOTE TO TOO/OUTVILIZ	(1.01.0.101.2001011.12)
		and Pentium OverDrive			ĺ
		with MMX technology			
		for 75/50, 90/60, and			
		100/66 available			
		March 1997			
		IVIAICII 1997	ı		

PC Processors (Pentium - MMX)

	Pentium [®] Processor with MMX™ Technology	Pentium Processor with MMX Technology			
Code name	P55C	P55CLM	P55CSLM/Tillamook		
/endor	Intel®	Same	Same		
ositioning	Desktopsystems	Notebook systems	Same		
nstruction architecture		Same	Same		
MMX technology	Yes / 57 new instructions	Same	Same		
.1 cache	16KB data; 16KB instruction	Same	Same		
1 cache - write policy	Write-back or thru (data)	Same	Same		
	Write-thru (instruction)				
•	4 way set associative (both)	Same	Same		
1 cache - parity	Parity in cache	Same	Same		
Parity	Parity on all external data and address transfers	Same	Same		
Execution units	2 fixed point units and	Same	Same		
	1 floating point unit	Same	Same		
Superscalarissue	2 integers per cycle or	Same	Same		
5.000.0. 10000	2 floating point per cycle	Same	Same		
Superscalar execution	2 integers per cycle or	Same	Same		
Japonoodidi CAGCULIOIT	2 floating point per cycle	Same	Same		
Out-of-order instruct	No	Same	Same		
Branch prediction	Dynamic (based on history); improved over P54C	Same			
·	and P54CS		Same		
Speculative execution		Same	Same		
Math coprocessor	Pipelined math coprocessor	Same	Same		
nternal processing	32-bits	Same	Same		
External data bus	64-bits	Same	Same		
External address bus	32-bits	Same	Same		
Vord size	32-bits	Same	Same		
Jser registers	8 GPR, 8 FP stack	Same	Same		
Cache line size	32 bytes	Same	Same		
Burst mode bus	Addr-data-data-data	Same	Same		
Power management	System Management Mode (SMM)	Same	Same		
Multiple processors	Multiple processor ready via built in APIC	Same	Same		
Die area	141 sq mm	Same	95 sq mm		
Technology	0.35u CMOS	Same	0.25u CMOS		
Supply voltage	2.8 volts internal / 3.3 v external	2.45 volts internal / 3.3 volts ext	1.8 volts internal / 2.5 volts ext		
Supply voltage	2.0 voits internal / 5.5 v external	2.45 Voits internal / 5.5 Voits ext	266: 2.0 volts internal / 2.5 v ext		
Power	16 watts max at 200 MHz; 17 watts for 233MHz	8 watts max at 166MHz	3.9 watts max at 233MHz		
Fransistors	4.5 million	Same	Same		
Package	273 pin grid array (PGA)	Tape Carrier Package (TCP) or	Tape Carrier Package (TCP) or		
	Pin compatible with non-MMX Pentiums except different core voltage	Mobile Module	280-pin Mobile Module (MMC1)		
Available date	January 1997 for 166, 200;	January 1997 for 150, 166MHz;	Sept 1997 for 200, 233MHz;		
	June 1997 for 233MHz	May 1997 for 133MHz	January 1998 for 166, 266MHz;		
requency	166/66, 200/66, 233/66MHz	133/66,150/60,166/66MHz	January 1999 for 300MHz 166/66, 200/66, 233/66, 266/66,		
OverDrive [®] upgrade	None	None	and 300/66MHz None		
Frequency OverDrive [®] upgrade	,		166/66, 200/66, 233/66, 2 and 300/66MHz		

PC Processors (Pentium Pro)

Pentium® Pro		
Code name	P60 (.6 micron); P6S (.35 micron)	
Vendor	Intel® /	
Positioning	Strong performance;	
	Software compatibility	
Instruction architecture	CISC/RISC/micro-ops	
L1 cache - size	8KB data; 8KB instruction	
L1 cache - write policy	Write-back or thru (data)	
	Write-thru (instruction)	
L1 cache - organization	4 way set associative (data)	
1.4	2 way set associative (instruction)	
L1 cache - parity	Parity in cache and internal registers	
L2 cache - size	256KB or 512KB or 1MB (external die)	
L2 cache - write policy	Write-through or write-back (programmable per line)	
L2 cache - organization	4 way set associative	
L2 cache - bus	On dedicated full speed bus / 64-bit path	
L2 cache - parity	Error Checking and Correcting (ECC)	
Parity - external bus	ECC on data bus; parity on	
_	address bus (frontside)	
Features	Nonblocking cache hierarchy	
	Independent backside and frontside buses operate	
Memory bus	concurrently 8 entry transactional buffer for memory bus	
Execution units	2 integer units; 1 floating point unit;	
	1 load unit; 1 store unit	
Pipeline stages	Decoupled, 14 stage superpipelined	
Superscalar dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	
Superscalarretire	3 micro-ops per cycle	
Out-of-order instructions	Yes (called dynamic execution)	
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically	
Constitution and system	predicts 10 to 15 nested branches	
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)	
Math coprocessor	Pipelined math coprocessor	
·		
Internal processing	32-bits	Nonblocking cache hierarchy - 486 and Pentium
External data bus	64-bits	are blocking; meaning an L2 cache miss causes
External address bus Word size	36-bits (address 64GB) 32-bits	processor to stall. P6 does not stall on an L2 cache
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	miss, but can do other useful work
Oddi registers	o or re, or re, to more or re via register remaining	Frantaida hua aytarnal 64 hit mamaruhua
Cache line size	32 bytes (8 bytes x 4 chunks)	Frontside bus - external 64-bit memory bus
Burst mode bus	Addr-data-data-data	Backside bus - 64-bit bus to integrated L2 cache
_	0	
Power management	System Management Mode (SMM)	Transaction buffer - while the Pentium Pro is
Multiple processors	Multiple processor ready via built in APIC	waiting for a memory access to complete, it can
Die area	306 (150) or 197 sg mm (CPU); 202 or 242 sg mm (L2)	begin another access. As many as 8 of these
Technology	0.6u (150), 0.35u (others); four layer metal BiCMOS	transactions can be outstanding
Supply voltage	2.9 volts	Minns and decades have believe 0100
Power (typical/maximum)	23/29 watts (150MHz)	Micro-ops - decoders break down CISC
Transistors	5.5 million in core + 15.5 (256) or 31 (512) million in L2	instructions into simpler operations that resemble RISC instructions. Micro-ops are easier to dispatch
Package	387 pin dual cavity PGA	and execute in parallel than their complex x86
Available date	late 1995; mid 1996 for 200MHz with 512KB	counterparts
_	August 1997 for 200MHz with 1MB	- Commonweal
Frequency	150/60, 180/60, 200/66MHz with 256KB L2 cache;	x86 instructions (8 to 120 bits long) go through three
	166/66, 200/66MHz with 512KB L2 cache;	parallel decoders to translate into single micro-ops
Doufouss a -	200/66 MHz with 1MB L2 cache	(complex ones into 1 to 4 micro-ops). Micro-ops are
Performance	327 SPECint92; 7.29 SPECint95 at 180MHz;	118 bits long
OverDrive® upgrade	220 SPECfp92; 6.08 SPECint95 at 180MHz 150, 180MHz support Pentium II OverDrive at 300MHz	
c.c.biiro apgiado	166, 200MHz support Pentium II OverDrive at 333MHz	
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PC Processors (Mobile Pentium II)

Mobile Pentium [®] II			
Code name Vendor Positioning Instruction architecture MMX technology	Deschutes Intel® Mobile systems CISC/RISC/micro-ops Yes / 57 new instructions / eight 64-bit MMX registers	Dixon Same Same Same Same	The "PE" is added to the 266PE and 300PE to distinguish these speeds from the half speed 512KB L2 cache versions.
L1 cache - controller L1 cache - size L1 cache - write policy L1 cache - organization L1 cache - bus L1 cache - parity	Integrated 16KB data; 16KB instruction Write-back or thru (data); write-thru (instruction) 4 way set associative (data); 2 way set associative (instruction) 64-bit / full speed / non-blocking Parity in cache and internal registers	Same Same Same Same Same Same	
L2 cache - controller L2 cache - size L2 cache - write policy L2 cache - organization L2 cache - bus L2 cache - type	Integrated 512KB / unified (external die) Write-through or write-back (programmable per line) 4 way set associative / non-blocking Half speed bus (or 1/3 speed) / 64-bit path Non-blocking / pipelined burst synchronous ECC	Same Same Full speed Same	d bus (or 1/3 speed) / 64-bit path
L2 cache - parity System bus - speed System bus - parity System bus - features Bus architecture	66MHz ECC on system bus; parity on address bus (frontside) Nonblocking cache hierarchy 8 entry transactional buffer for system bus Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)	Same Same Same Same Same Same	Nonblocking cache hierarchy - 486 and Pentium are blocking; meaning an L2 cache miss causes processor to stall. Pentium II does not stall on an L2 cache miss, but can do other useful work Frontside bus - external 64-bit memory (system) bus
Superscalar issue Superscalar retire	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) / 512 entry BTB / typically	Same Same Same Same Same Same Same	Backside bus - 64-bit bus to integrated L2 cache Transaction buffer - while the Pentium II is waiting for a memory access to complete, it can begin another access. As many as 8 of these transactions can be outstanding
Speculative execution Math coprocessor	predicts 10 to 15 nested branches Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches) Pipelined math coprocessor	Same Same	Micro-ops - decoders break down CISC instructions into simpler operations that resemble RISC instructions. Micro-ops are easier to dispatch and execute in parallel
Internal processing External data bus External address bus Word size User registers Cache line size Burst mode bus Power management Multiple processors	32-bits (300 bit internal bus width) 64-bit system bus with ECC 36-bits (64GB physical address space; 64TB virtual) 32-bits 8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) Addr-data-data-data-data System Management Mode (SMM) Not supported	Same Same Same Same Same Same Same Same	than their complex x86 counterparts x86 instructions (8 to 120-bits long) go through three parallel decoders to translate into single micro-ops (complex ones into 1 to 4 micro-ops). Micro-ops are 118 bits long
Technology CPU voltage	0.25u; five layer metal CMOS 1.6 volts (3.3 volt I/O)	0.25u; 40 0	DMHz is 0.18u and 0.25u 2.5 volt I/O); 1.5v for 266MHz low voltage 000MHz
Power (total in watts)	8.6 watts (supports QuickStart allowing 0.4 watt idle power state)	366MHz: 266MHz lo	9.5 watts; 6.6 watts typical (5.8 watts for ow voltage); supports QuickStart allowing le power state
Transistors Package type	~7.5 million 280-pin Mobile Module (MMC1) 400-pin Mobile Module (MMC2) 240-pin Mini-cartridge	280-pin M 400-pin M 240-pin N Ball Grid	n (366MHz) lobile Module (MMC1) obile Module (MMC2) lini-cartridge Array (BGA)
Available date	April 1998 (233 and 266MHz); September 1998 (300MHz)	1	999; April 1999 (266MHz low voltage);
Frequency (clock/system)	233/66MHz with half speed L2 cache bus 266/66MHz with half speed L2 cache bus 300/66MHz with half speed L2 cache bus	266/66MH 266PE/66 300PE/66 333/66MH	0 (400MHz) Iz <u>low voltage</u> with full speed L2 bus MHz with full speed L2 cache bus MHz with full speed L2 cache bus Iz with full speed L2 cache bus Iz with full speed L2 cache bus Iz with full speed L2 cache bus
Chipset support	440BX	400/66MH 440BX, 44	Iz with full speed L2 cache bus IOMX

PC Processors (Pentium II)

Pentium® II		
Code name	Klamath	Deschutes
Vendor	Intel®	Same
Positioning	Desktop systems; entry servers	Same
Instruction architecture	CISC/RISC/micro-ops	Same
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers	Same
L1 cache - controller	Integrated	Same
L1 cache - size	16KB data; 16KB instruction	Same
L1 cache - size L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	Same
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)	
L1 cache - bus	64-bit / full speed	Same
L1 cache - type	Non-blocking	Same
L1 cache - parity	Parity in cache and internal registers	Same
L2 cache - controller	Integrated	Same
L2 cache - controller	512KB / unified (external die)	Same
L2 cache - write policy	Write-through or write-back (programmable per line),	Same
LZ dadrie Write policy	uncacheable, write-protect	Came
L2 cache - organization	4 way set associative / non-blocking	Same
L2 cache - bus	Dedicated 1/2 or 1/3 speed bus / 64 bit path	Same
L2 cache - type	Non-blocking / pipelined burst synchronous	Same
L2 cache - parity	Non-ECC or ECC on 233 and 266MHz / ECC on all 300MHz	ECC
System bus - parity	ECC on system bus; parity on address bus (frontside)	Same
System bus - speed	66MHz	66 or 100MHz
System bus - features	Nonblocking cache hierarchy	Same
System bus - leatures	8 entry transactional buffer for system bus	Same
Bus architecture	Independent backside and frontside buses operate	Same
Dus architecture	concurrently / Dual Independent Bus Architecture (DIB)	Jame
For each and the	O later and MANY and the Affection and the site of the later and the site of t	0
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit	
Pipeline stages	Decoupled, 14 stage superpipelined	Same
Supscardispatch/execute Superscalar issue	5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical)	Same Same
Superscalar issue Superscalar retire	3 micro-ops per cycle (3 micro-ops is typical)	Same
•	Yes (called dynamic execution)	Same
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically	Same
Dianorprodiction	predicts 10 to 15 nested branches	Game
Speculative execution	Yes (typically 20 to 30 instructions beyond counter	Same
	with an average of 5 branches)	
Math coprocessor	Pipelined math coprocessor	Same
Internal processing	32-bits (300 bit internal bus width)	Same
External data bus	64-bit system bus with ECC	Same
External address bus	36-bits (4 GB physical address space; 64 TB virtual)	Same
Word size	32-bits	Same
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	Same
Cache line size	32 bytes (8 bytes x 4 chunks)	Same
Burst mode bus	Addr-data-data-data	Same
Power management	System Management Mode (SMM)	Same
Multiple processors	Glueless 2 way SMP via built in APIC	Same
Die area	203 sq mm (CPU) / 560 mils/side	131 sq mm (CPU) / ~429 x 474 mils/side
Technology	0.35u; four layer metal CMOS	0.25u; five layer metal CMOS
CPU voltage	2.0 or 2.8 volts	2.0 volts
•	33.6/34.8 (233MHz), 37.0/38.2 (266), 41.4/43.0 (300)	19.4/23.6 (333 MHz), 20.2/24.5 (350), 26.7/27.9 (400)
Transistors	~7.5 million	Same
Package type	Single Edge Contact Cartridge (SECC) requires Intel Slot 1	SECC or SECC2 requires Intel Slot 1
Package size (of SEC)	5.505 inches x 2.473 inches x 0.647 inches	Same
Available data	528 pin plastic land-grid array (LGA) package	Same
Available date	Apriil 1997 (233 and 266MHz); August 1997 (300MHz)	January 1998 (333MHz); April 1998 (350, 400MHz) August 1998 (450MHz)
Frequency (clock/system)	233/66MHz with 117MHz L2 cache bus	333/66MHz with 166MHz L2 cache bus
(3.00.00)	266/66MHz with 133MHz L2 cache bus	350/100MHz with 175MHz L2 cache bus
	300/66MHz with 150MHz L2 cache bus	400/100MHz with 200MHz L2 cache bus
		450/100MHz with 225MHz L2 cache bus
Chipset support	440FX,440LX	440FX, 440LX, 440BX, 440GX

PC Processors (Pentium II Xeon)

Pentium [®] II Xeon™	
Code name	Deschutes Slot 2 or DS2P Intel®
Vendor Positioning	
Instruction architecture	Mid-range and higher servers and workstations CISC/RISC/micro-ops
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers
LA cook of cooking the co	lette mede d
L1 cache - controller	Integrated
L1 cache - size	16KB data; 16KB instruction
L1 cache - write policy L1 cache - organization	Write-back or thru (data); write-thru (instruction) 4 way set associative (data); 2 way set associative (instruction)
L1 cache - bus	64-bit / full speed
L1 cache - type	Non-blocking
L1 cache - parity	Parity in cache and internal registers
L 2 acaba acastrollar	Integrated
L2 cache - controller	Integrated 513/FP 1MP or 2MP (unified (outerpal dia) (CSPAM)
L2 cache - size L2 cache - write policy	512KB, 1MB, or 2MB / unified (external die) / CSRAM Write-through or write-back (programmable per line),
LZ cache - write policy	uncacheable, write-protect
L2 cache - organization	4 way set associative / non-blocking
L2 cache - bus	Dedicated full speed bus / 64-bit path
L2 cache - type	Non-blocking / pipelined burst synchronous
L2 cache - parity	ECC
System bus - parity	ECC on system bus; parity on address bus (frontside)
System bus - speed	100MHz
System bus - features	Nonblocking cache hierarchy
-,	8 entry transactional buffer for system bus
Bus architecture	Independent backside and frontside buses operate
	concurrently / Dual Independent Bus Architecture (DIB)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Pipeline stages	Decoupled, 14 stage superpipelined
	5 micro-ops per cycle (3 micro-ops is typical)
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically
	predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter
Moth conrecesor	with an average of 5 branches) Pipelined math coprocessor
Math coprocessor	ripelined matricoprocessor
Internal processing	32-bits (300-bit internal bus width)
External data bus	64-bit system bus with ECC
External address bus	36-bits (64GB physical address space (PSE-36); 64TB virtual)
Word size	32-bits
User registers Cache line size	8 GPR, 8 FP, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks)
Burst mode bus	Addr-data-data-data
Power management	System Management Mode (SMM)
Systems management	SMBus for thermal sensor, PIROM, Scratch EEPROM
Multiple processors	1-, 2-, 4-, and 8-way SMP support
Die area	131 sq mm (CPU), 560 mils/side / 222 sq mm (L2 cache)
Technology	0.25u; five layer metal CMOS
CPU voltage	1.8 to 2.8 volts
Transistors	~7.5 million
Package type	Single Edge Contact (SEC) cartridge requires Intel Slot 2 (SC330)
Package size (of SEC)	4.992 inches high x 6.000 inches wide x 0.733 inches
Available date \(\)	July 1998 (400MHz), October 1998 (450MHz)
Frequency	400/100MHz with 400MHz L2 cache bus and 512KB L2 cache
	400/100MHz with 400MHz L2 cache bus and 1MB L2 cache
	450/100MHz with 450MHz L2 cache bus and 512KB L2 cache
	450/100MHz with 450MHz L2 cache bus and 1MB L2 cache
Chineateunnart	450/100MHz with 450MHz L2 cache bus and 2MB L2 cache
Chipset support	450NX (servers) or 440GX (workstations)

Intel® Pentium® III for des MHz	sktop and entry servers 450,500, 550,600	533B, 600B	500E, 550E	600E, 650, 700, 750, 800, 850, 1.0GHz	533EB, 600EB, 667, 733, 800EB, 866, 933, 1.0BGHz, 1.13GHz
Code name Instruction architecture MMX™ / Streaming SIMD	Katmai CISC/RISC/micro-ops MMX (57 new instructions) / Stream	aming SIMD Extension	Coppermine (or Co	ppermine-T)	
L1 cache - bus L1 cache - size/controller L1 cache - write policy L1 cache - organization	64-bit / full speed 16KB data; 16KB instruction / inte Write-back or thru (data); write-th 4 way set associative (data); 2 wa	ru (instruction)	ruction)		
L2 cache - size L2 cache - data path L2 cache - buffering	512KB / half speed 64-bit data path / ECC None			quad-wide cache ling of read and stores with 4 writeback buff	e / ECC (called Advanced
L2 cache - organization L2 cache - controller L2 cache - write policy L2 cache - type	4-way set associative Integrated / unified (external die) Write-through or write-back (prog Non-blocking / pipelined burst syr	rammable per line), und	8-way set associativ Integrated / unified (i	e ´ nternal die; on die)	
System bus - speed Memory addressability System bus - width System bus - parity	100MHz 4GB memory addressability 64-bit system bus with ECC ECC on system bus; parity on ad	133MHz dress bus (frontside bu	100MHz 64GB memory addres	100MHz essability	133MHz
Execution units Supscal dispatch/execute Superscalar issue Superscalar retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating po 5 micro-ops per cycle (3 micro-op 6 micro-ops per cycle (3 micro-op 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) / 512 predicts 10 to 15 nested brand Yes (typically 20 to 30 instruction with an average of 5 branches Pipelined math coprocessor	es is typical); Pipeline st os is typical) entry BTB / typically ches s beyond counter	B = 133MHz Froi E = 256KB full sp with <u>Advance</u> L2 cache bus also	ntside Bus (system b	us) to main memory nced Transfer Cache s
Serial number Bus architecture Internal processing User registers Cache line size Power management	Unique processor serial number Independent backside and frontsi 32-bits (300 bit internal bus width 8 GPR, 8 FP, 8 FPscalar and SIM 32 bytes (8 bytes x 4 chunks); bu System Management Mode (SMM Glueless 2-way SMP via built in A	ide buses operate conc) /ID, 40 more GPR via re rst mode bus of addr-da //)	egister renaming ata-data-data	ndent Bus Architectu	
Multiple processors Technology (micron)	0.25u	0.25u	0.18u	0.18u	0.18u
Transistors Package type Connector	~9.5 million for processor core Single Edge Contact Cartridge Single Edge Contact Cartridge		~28.1 million FC-PGA (Flip-Chip Pin Grid Array)	or Flip-Chip Pin G	~28.2 million act Cartrdg 2 (SECC2) rid Array (FC-PGA)
Available date	Requires Intel Slot 1 March 1999 (450 and 500MHz), May 1999 (550MHz), August 1999 (600MHz)	Requires Intel Slot 1 September 1999	Socket 370 October 1999	(800, 800EB, 1 and Requires Intel Slot October 1999, Dec 1999 (750, 800) Mar 2000 (850), Jun 2001 (1.0, 1.1)	1.13GHz only SECC2) 1 or Socket 370 October 1999, Dec 1999 (800EB), Mar 2000 (866), Mar 2000 (1.0GHz) May 2000 (933) July 2000 (1.13GHz)
Frequency (MHz)	450 with 100MHz FSB 500 with 100MHz FSB 550 with 100MHz FSB 600 with 100MHz FSB	533B with 133 FSB 600B with 133 FSB	500E with 100 FSB 550E with 100 FSB	600E w/ 100 FSB 650 with 100 FSB 700 with 100 FSB 750 with 100 FSB 800 with 100 FSB 1.0 with 100 FSB 1.1 with 100 FSB	533EB with 133 FSB 600EB with 133 FSB 667 with 133 FSB 733 with 133 FSB 800EB with 133 FSB 933 with 133 FSB 1.0BGHz with133FSB 1.13GHz with133FSB
Chipset support	440BX, 440GX, 810, 810E, 820, 840	810E, 820, 840	440BX,440GX, 810x,815x,820x, 840	440BX, 440GX, 810x, 815x, 820x, 840	810x, 815x, 820x, 840

Intel® Pentium® III for desktop and entry-level workstations and servers

Code name Tualatin (pronounced "TWO-ala-tin")
Instruction architecture IA-32 / CISC/RISC/micro-ops

MMX™/Streaming SIMD MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)

L1 cache - bus 64-bit / full speed

L1 cache - size/controller 16KB data; 16KB instruction / integrated / non-blocking L1 cache - write policy Write-back or thru (data); write-thru (instruction)

L1 cache - organization 4 way set associative (data); 2 way set associative (instruction)

L2 cache - size

256 or 512KB / full speed (Advanced Transfer Cache)
L2 cache - data path
L2 cache - buffering

256-bit data path / quad-wide cache line / ECC
Intelligent buffering of read and stores (called Advanced

System Buffering with 4 writeback buffers, 6 fill buffers,

8 bus queue entries)
on 8-way set associative

L2 cache - organization 8-way set associative
L2 cache - controller Integrated / unified (internal die; on die)

L2 cache - write policy Write-through or write-back (programmable per line), uncacheable, write-protect

L2 cache - type Non-blocking / pipelined burst synchronous

Frontside bus - speed 133MHz

Memory addressability
System bus - width

64GB memory addressability
64-bit system bus with ECC

System bus - parity ECC on system bus; parity on address bus (frontside bus)

Execution units 2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit

Supscal dispatch/execute 5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined

Superscalar issue 6 micro-ops per cycle (3 micro-ops is typical)

Superscalar retire 3 micro-ops per cycle

Out-of-order instructions Yes (called dynamic execution)

Branch prediction Dynamic (based on history) / 512 entry BTB / typically

predicts 10 to 15 nested branches

Yes (typically 20 to 30 instructions beyond counter

with an average of 5 branches)
Math coprocessor
Pipelined math coprocessor

Processor serial number None

Speculative execution

Serial number Unique processor serial number

Bus architecture Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)

Internal processing 32-bits (300 bit internal bus width)

User registers 8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming Cache line size 32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data

Power management System Management Mode (SMM)

Multiple processors Some support 2-way SMP with appropriate chipset support

Technology (micron) 0.13u

Package type Flip-Chip Pin Grid Array-2 (FC-PGA2)
Connector Requires Socket 370 (PGA370)

Frequency (MHz) 900 MHz Ultra Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers (announced Jan 2003)

933 MHz Low Voltage with 512KB L2 cache for blade servers (announced September 2002)

1.0A GHz 256KB L2 cache for desktop, entry-level workstations and servers (announced August 2001)
 1.0 GHz Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers (announced January 2003)
 1.13A GHz 256KB L2 cache for desktop, entry-level workstations and servers (announced August 2001)

L2 cache bus also called Backside Bus

Memory or system bus also called Frontside Bus

1.13 GHz-S 512KB L2 cache for servers (announced June 2001)

1.20 GHz 256KB L2 cache for desktop, entry-level workstations and servers (announce August 2001)

1.26 GHz-S 512KB L2 cache for servers (announced August 2001)

1.4 GHz-S 512KB L2 cache for servers and blade servers (announced January 2002)

Chipset support Intel 815x, 820x, 840 and others ServerWorks® HE-SL and others

Server blade support Pentium III at 933MHz and 1.4GHz supported in "Performance Server Blades"

Intel® Mobile Pentium® III	l	
Code name Positioning Instruction architecture MMX™/Streaming SIMD	Coppermine Mobile systems CISC/RISC/micro-ops MMX (57 new instructions) / Streaming SIMD Extensions (70 new instruction	ıs)
L1 cache - bus L1 cache - size/controller L1 cache - write policy L1 cache - organization	64-bit / full speed 16KB data; 16KB instruction / integrated / non-blocking Write-back or thru (data); write-thru (instruction) 4 way set associative (data); 2 way set associative (instruction)	
L2 cache - size L2 cache - data path L2 cache - buffering L2 cache - organization L2 cache - controller L2 cache - write policy L2 cache - type	256KB / full speed (Advanced Transfer Cache) 256-bit data path / quad-wide cache line / ECC Intelligent buffering of read and stores (called Advanced System Buffering with 4 write-back buffers, 6 fill buffers, 8 bus queue entries) 8-way set associative Integrated controller / unified L2 cache (internal die; on die) Write-through or write-back (programmable per line), uncacheable, write-prof Non-blocking / pipelined burst synchronous	
System bus - speed System bus - width System address bus System bus - parity	100MHz Frontside Bus 64-bit system bus with ECC 36-bits (4GB memory cacheability; 64GB memory addressability) ECC on system bus; parity on address bus (frontside bus)	Non-blocking cache hierarchy - 486 and Pentium are blocking; meaning an L2 cache miss causes processor to stall. Pentium II and III do not stall on an
Execution units Pipeline stages Supscal dispatch/execute Superscalar issue Superscalar retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit Decoupled, 14 stage superpipelined 5 micro-ops per cycle (3 micro-ops is typical) 6 micro-ops per cycle (3 micro-ops is typical) 3 micro-ops per cycle Yes (called dynamic execution) Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches Yes (typically 20 to 30 instructions beyond counter; ave of 5 branches) Pipelined math coprocessor	L2 cache miss, but can do other useful work Frontside bus - external 64-bit memory (system) bus Backside bus - 256-bit bus to integrated L2 cache Transaction buffer - while the Pentium II and Pentium III are waiting for a memory access to complete, it can
Serial number Bus architecture Internal processing User registers Cache line size Burst mode bus Multiple processors	Unique processor serial number Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB) 32-bits (300 bit internal bus width) / 32-bit word size 8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming 32 bytes (8 bytes x 4 chunks) Addr-data-data-data None	begin another access. As many as 8 of these transactions can be outstanding SpeedStep - processor operates at full speed in Maximum Performance Mode (on AC power) and reduced speed in Battery Optimized Mode (on battery)
Technology (micron) CPU voltage Power management	0.18u 1.1-1.7 volts (2.5 volt I/O); 1.6v typical (except 1.35v for some low-power ver 500MHz Ultra Low Voltage is 1.1v typical (0.975v battery optimized) QuickStart and Deep Sleep modes for low-power dissipation	rsions);
Transistors Package type Available date Frequency (MHz)	~28.1 million 400-pin Mobile Module (MMC2), 240-pin Mini-cartridge, Ball Grid Array (Oct 1999 for 400, 450, 500MHz; Jan 2000 for 500MHz (1.35v), 600, 650MHz (1.35v), 750MHz; Sept 200 for 800 and 850MHz; Jan 2001 for 500MHz (1.1v) Mar 2001 for 900MHz and 1GHz; May 2001 for 600MHz (1.1v) and 750MHz 400MHz 450MHz 500MHz 500MHz Low Voltage (1.35v) 500MHz Ultra Low Voltage (1.1v) (with Intel SpeedStep™ tech); 300MHz in 600MHz (with Intel SpeedStep™ technology); 500MHz in Battery Optimized 600MHz (with Intel SpeedStep technology); 500MHz in Battery Optimized 700MHz Low Voltage (1.35v) (with Intel SpeedStep technology); 500MHz in Battery Optimized 700MHz Low Voltage (1.35v) (with Intel SpeedStep technology); 500MHz in Battery Optimized 750MHz (with Intel SpeedStep technology); 550MHz in Battery Optimized 750MHz (with Intel SpeedStep technology); 600MHz in Battery Optimized 850MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized 800MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized 800MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized 800MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized 800MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized 800MHz (with Intel SpeedStep technology); 700MHz in Battery Optimized	in Battery Optimized Mode (0.975v) and Battery Optimized Mode (0.975v) and Battery Optimized Mode (0.975v) and Mode attery Optimized Mode (0.975v) and Mode attery Optimized Mode attery Optimized Mode (1.1v) and Mode by in Battery Optimized Mode (1.1v) by Mode attery Optimized Mode (1.1v) by Mode by In Battery Optimized Mode (1.1v) by Mode b
Chipset support	440BX, 440MX, 440ZX-M, 815EM	

Mobile Intel® Pentium® III	Processor-M for mobile sys	tems (and s	server blade systems)			
Code name Instruction architecture MMX [™] / Streaming SIMD Technology	Tualatin (pronounced "TWO-IA-32 / CISC/RISC/micro-ops MMX (57 new instructions) / S Enhanced Intel SpeedStep™ t	Streaming S	IMD Extensions (70 new ins	structions)		
L1 cache - bus L1 cache - size/controller L1 cache - write policy L1 cache - organization	64-bit / full speed 16KB data; 16KB instruction / integrated / non-blocking Write-back or thru (data); write-thru (instruction) 4 way set associative (data); 2 way set associative (instruction) L2 cache bus also called Backside Bus Memory or system bus also called Frontside Bus					
L2 cache - size L2 cache - data path L2 cache - buffering L2 cache - organization L2 cache - write policy	256-bit data path / quad-wid Intelligent buffering of read an 8 bus queue entries) / Data Po 8-way set associative / non-bl	512KB / full speed (Advanced Transfer Cache) / integrated / unified (internal die; on die) 256-bit data path / quad-wide cache line / ECC Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) / Data Prefetch Logic 8-way set associative / non-blocking / pipelined burst synchronous Write-through or write-back (programmable per line), uncacheable, write-protect				
Frontside bus - speed Memory addressability System bus - width System bus - parity	133MHz (some at 100MHz) 64GB memory addressability 64-bit system bus with ECC	33MHz (some at 100MHz) 4GB memory addressability				
Execution units Supscal dispatch/execute Superscalar issue/retire Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer/MMX units; 1 floating 5 micro-ops per cycle (3 micro- Issues 6 micro-ops per cycle Yes (called dynamic executio Dynamic (based on history) / Yes (typically 20 to 30 instruct Pipelined math coprocessor	o-ops is typi (3 micro-op n) 512 entry B	cal); Pipeline stages: decou s is typical) / retires 3 micro TB / typically predicts 10 to	ops per cycle 15 nested branches	pelined	
Serial number Bus architecture Internal processing User registers Cache line size Power management Multiple processors	Unique processor serial numb Independent backside and fro 32-bits (300 bit internal bus wi 8 GPR, 8 FP, 8 FPscalar and 32 bytes (8 bytes x 4 chunks). Quick Start, Deep Sleep, Dee No SMP support (2-way SMP	ontside buse idth) SIMD, 40 n ; burst mode per Sleep	nore GPR via register renar e bus of addr-data-data-dat	ning a	, ,	
Technology (micron) Package type	0.13u (130-nanometer) Micro-FCPGA (Flip-Chip Pin Micro-FCBGA (Flip-Chip Ball					
Frequency (MHz)	700MHz Ultra Low Voltage* 733MHz Low Voltage 750MHz Ultra Low Voltage 750MHz Low Voltage 800A MHz Low Voltage 800MHz Low Voltage** 800MHz Ultra Low Voltage* 800MHz Ultra Low Voltage* 850MHz Ultra Low Voltage 850MHz Ultra Low Voltage 866MHz Ultra Low Voltage 866MHz Ultra Low Voltage 900MHz Ultra Low Voltage 933MHz Ultra Low Voltage 933MHz Ultra Low Voltage 933MHz Ultra Low Voltage 933MHz Low Voltage 931MHz Low Voltage 131MHz 1GHz 1CHZ 1CHZ 1.13GHz 1.26GHz 1.33GHz	133MHz 100MHz 100MHz 100MHz 133MHz 100MHz 133MHz 133MHz 133MHz 133MHz 133MHz 133MHz	Maximum Performance Mode 700MHz at 1.1V 733MHz at 1.15V 750MHz at 1.15V 800MHz at 1.15V 860MHz at 1.1V 866MHz at 1.1V 966MHz at 1.1V 933MHz at 1.15V 933MHz at 1.15V 1.06GHz at 1.40V 1.13GHz at 1.40V 1.2GHz at 1.40V 1.2GHz at 1.40V 1.2GHz at 1.40V 1.2GHz at 1.40V	Battery Optimized Mode 300MHz at 0.95V 466MHz at 1.05V 350MHz at 1.05V 500MHz at 1.05V 533MHz at 1.05V 400MHz at 0.95V 400MHz at 0.95V 400MHz at 0.95V 400MHz at 1.15V 733MHz at 1.15V 800MHz at 1.15V 800MHz at 1.15V 800MHz at 1.15V	Announce date October 2001/Nov 2001* October 2001 January 2002 October 2001 October 2001 October 2001/Mar 2002** April 2002* April 2002* January 2002 September 2002 January 2002 July 2001 September 2002 January 2003 January 2003 January 2003 January 2003 Japuary 2001 July 2001 July 2001 September 2002 July 2001 September 2002 July 2001 September 2002 July 2001 September 2002 September 2002 September 2002 September 2002 September 2002 September 2002	
Chipset support Server blade support	Intel 830MP, 830M, 830MG at * Supported in server blade ** Announced March 2002 f systems with ServerWorl	nd others systems; I or server b	Micro-FCBGA only; uses I lade systems; Micro-FCB	ntel 440GX chipset	·	

Mobile Intel® Pentium® 4	Processor-M for mobile systems		
Code name Micro-architecture MMX™ / Streaming SIMD SSE2 Hyper-Threading Power mgmt technology	Mobile Northwood IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) (To new instructions) / Streaming SIMD Extensions (To new instructions) / Streaming SIMD Extensions 2 (144 new instructions) / Some: Hyper-Threading (HT) Technology (hardware support for multi-threaded applied Enhanced Intel SpeedStep™ technology, Stop Grant, Sleep, Deep Sleep, Deeper Sleep / Deeper Sl	ications)	
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)	ed	
L2 cache - size L2 cache - data path L3 cache	512KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (sectors) / 8-way set associative / integrated / unified (internal die; on die) None	usually divided into two	o 64 byte
System bus Memory addressability System bus - width	400 or 533MHz (transfers data four times per clock) / address bus transfers at two tir 64GB memory addressability / 36-bit addressing / address bus is double clocked at 2 64-bit data path		e cache line size
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid B Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers	Execution Engine)	
Compatibility Multiple processors	Compatible with IA-32 software No SMP support		
Technology (micron) Package and connector	 0.13u 400MHz: Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mosocket 533MHz: Micro Flip-Chip Pin Grid Array (uFCPGA2) requires 478-pin surface mosocket 		
Frequency (MHz)	bus Mode 1.4GHz 400MHz 1.4GHz at 1.3 volts 1.2GHz at 1.2v (<2 watts avg power)	with Hyper-Threading with Hyper-Threading	date April 2002 April 2002 March 2002 March 2002 April 2002 June 2002 June 2002 Sept 2002 Jan 2003 April 2003 June 2003 June 2003 June 2003 June 2003 June 2003 Sept 2003 Sept 2003 Sept 2003 Sept 2003 Sept 2003 Sept 2003
Chipset support	Intel 845MZ with DDR-SDRAM memory Intel 845MP with DDR-SDRAM memory Intel 852GM, 852GME, 852PM with DDR-SDRAM memory		

	ssor for mobile systems			
Code name Branding	Banias Part of the Intel Centrino™ mo Network Connection wireless	0,	cluded with an Intel 855 fa	amily chipset and Intel PRO/Wireless
SSE2	IA-32 / micro-op fusion, dedic D MMX™ (57 new instructions) of Streaming SIMD Extensions 2	ated stack manager, adv / Streaming SIMD Exten 2 (144 new instructions)	sions (70 new instructions	,
Power mgmt technology	Enhanced Intel SpeedStep™	technology, Auto Halt, S	top Grant, Deep Sleep, De	eeper Sleep
L1 cache - bus L1 data cache	256-bit data path / full speed 32KB data cache / integrated			
L1 instruction cache	32KB instruction cache / integrated	grated		
L2 cache - size L2 cache - data path L3 cache	1MB / full speed (Advanced T 256-bit data path (32 bytes) / None		8-way set associative / in	tegrated / unified (internal die; on die)
System bus Memory addressability System bus - width	400MHz (transfers data four t 64GB memory addressability 64-bit data path	. ,		s per clock / 64 byte cache line size d at 200MHz
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating poin Yes (out-of-order instruction e Dynamic (based on history) Yes (Advanced Dynamic Exec Pipelined floating point unit	xecution)	re unit	
Compatibility Multiple processors	Compatible with IA-32 softwa No SMP support	re		
Technology (micron) Package and connector	0.13u Micro Flip-Chip Pin Grid Arı (mPGA479M socket) or Micr			ount Zero Insertion Force (ZIF) socke surface mount (479-ball)
Frequency (MHz/GHz)		Highest Frequency Mode	Lowest Frequency Mode	Announce date
and available date	900MHz Ultra Low Voltage 1.0GHz Ultra Low Voltage 1.1GHz Ultra Low Voltage 1.1GHz Low Voltage 1.2GHz Low Voltage 1.3GHz Low Voltage 1.3GHz 1.4GHz 1.5GHz 1.6GHz 1.7GHz	900MHz at 1.0 volts 1.0GHz at 1.0 volts 1.1GHz at 1.0 volts 1.1GHz at 1.18 volts 1.2GHz at 1.18 volts 1.3GHz at 1.18 volts 1.3GHz at 1.5 volts 1.4GHz at 1.5 volts 1.5GHz at 1.5 volts 1.6GHz at 1.5 volts 1.7GHz at 1.5 volts	600MHz at 0.85 volts 600MHz at 0.85 volts 600MHz at 0.85 volts 600MHz at 0.96 volts	March 2003 June 2003 April 2004 (also Pentium M 713) March 2003 June 2003 April 2004 (also Pentium M 718) March 2003 March 2003 March 2003 March 2003 June 2003 June 2003

[Mobile] Intel Pentium M Processor 7xx

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	Pe	Clock speed rformance Mode	Clock speed Battery Mode	L2 cache	Execute Disable Bit	System bus	Technology	Available date
Intel Pentium M Processo	or Ultra Low Voltage 713	1.10GHz	600MHz	1MB	No	400MHz	130nm	April 2004
Intel Pentium M Processo	· ·	1.00GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processo	•	1.10GHz	600MHz	2MB	No	400MHz	90nm	July 2004
	or Ultra Low Voltage 733J	1.10GHz	600MHz	2MB	Yes	400MHz	90nm	August 2004
Intel Pentium M Processo	· ·	1.20GHz	600MHz	2MB	Yes	400MHz	90nm	January 2005
Intel Pentium M Processo	or Ultra Low Voltage 773	1.30GHz	600MHz	2MB	Yes	400MHz	90nm	January 2006
Intel Pentium M Processo	or Low Voltage 718	1.30GHz	600MHz	1MB	No	400MHz	130nm	April 2004
Intel Pentium M Processo	or Low Voltage 738	1.40GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processo	or Low Voltage 758	1.50GHz	600MHz	2MB	Yes	400MHz	90nm	January 2005
Intel Pentium M Processo	or Low Voltage 778	1.60GHz	600MHz	2MB	Yes	400MHz	90nm	July 2005
Intel Pentium M Processo	or 705	1.50GHz	600MHz	1MB	No	400MHz	130nm	July 2004
Intel Pentium M Processo		1.50GHz	600MHz	1MB	No	400MHz	130nm	November 200
Intel Pentium M Processo		1.40GHz	600MHz	2MB	No	400MHz	90nm	October 2004
ntel Pentium M Processo		1.50GHz	600MHz	2MB	No	400MHz	90nm	June 2004
ntel Pentium M Processo		1.50GHz	600MHz	2MB	No	400MHz	90nm	January 2005
ntel Pentium M Processo		1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2004
ntel Pentium M Processo		1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2005
ntel Pentium M Processo		1.60GHz 1.60GHz	800MHz	2MB			90nm	
					Yes	533MHz		January 2005
ntel Pentium M Processo		1.70GHz	600MHz	2MB	No Y oo	400MHz	90nm	May 2004
ntel Pentium M Processo		1.73GHz	800MHz	2MB	Yes	533MHz	90nm	January 2005
ntel Pentium M Processo		1.80GHz	600MHz	2MB	No	400MHz	90nm	May 2004
ntel Pentium M Processo		1.86GHz	800MHz	2MB	Yes	533MHz	90nm	January 2005
ntel Pentium M Processo		2.00GHz	600MHz	2MB	No	400MHz	90nm	May 2004
ntel Pentium M Processo		2.00GHz	800MHz	2MB	Yes	533MHz	90nm	January 2005
ntel Pentium M Processo	or 765	2.10GHz	600MHz	2MB	No	400MHz	90nm	October 2004
ntel Pentium M Processo	or 770	2.13GHz	800MHz	2MB	Yes	533MHz	90nm	January 2005
ntel Pentium M Processo	or 780	2.26GHz	800MHz	2MB	Yes	533MHz	90nm	July 2005
requires improved proce	essor cooling because of h	igher Thermal I	Design Power					
Code name	Dothan (705, 705a, 713,		,					
Branding	Part of the Intel Centrino	o™ mobile tecl	nnology when	included v	with an Intel	855 or 915	Express Chip	set family and
	Intel PRO/Wireless Netw	ork Connection	wireless chip					
Micro-architecture	IA-32 / micro-op fusion, o	dedicated stack	manager, adva	anced brai	nch prediction	on, power-or	otimized proc	essor system bus
MMAYTM / Strooming SIME	OMMX™ (57 new instruction	one) / Streaming						
viiviA····/ Streaming SilviL	TIVIIVIA (31 HOW III3H dolld	Jiis) / Sireaiiiiii	g SIMD Extens	ions (70 n			·	,
	Streaming SIMD Extension			ions (70 n			·	•
SSE2		ons 2 (144 new	instructions)		ew instructi	ons)	Sleep	•
SSE2 Power mgmt technology	Streaming SIMD Extensi	ons 2 (144 new	instructions)		ew instructi	ons)	Sleep	·
SSE2 Power mgmt technology Hyper-Threading	Streaming SIMD Extension Enhanced Intel SpeedS No	ons 2 (144 new Step™ technolo	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	·
SSE2 Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology ¹	Streaming SIMD Extension Enhanced Intel SpeedS	ons 2 (144 new Step™ technolo	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	,
SSE2 Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology ¹	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None	ons 2 (144 new step™ technolo data areas fron	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	,
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None	ons 2 (144 new step™ technolo data areas fror eed	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr	ons 2 (144 new step™ technolo data areas from eed ated	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None	ons 2 (144 new step™ technolo data areas from eed ated	instructions) egy, Auto Halt,	Stop Grar	ew instructi	ons)	Sleep	,
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr	ons 2 (144 new step™ technolo data areas from eed ated integrated	instructions) gy, Auto Halt, m malicious so	Stop Grar	ew instructi	ons)	Sleep	
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache /	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Trai	instructions) gy, Auto Halt, m malicious so	Stop Grar	new instructi	ep, Deeper		
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache /	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Trai	instructions) gy, Auto Halt, m malicious so	Stop Grar	new instructi	ep, Deeper		
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path L3 cache	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte) None	ons 2 (144 newstep™ technology data areas from eed ated integrated (Advanced Traites) / 64 byte ca	instructions) igy, Auto Halt, m malicious so insfer Cache) che line size /	Stop Gran	new instruction, Deep Sleecution	eep, Deeper	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path L3 cache System bus	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers	ons 2 (144 newstep™ technology data areas from eed ated integrated (Advanced Trailes) / 64 byte cases data 4 times process.	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size /	Stop Grar ftware exe 8-way set ress bus t	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal	ons 2 (144 newstep™ technology data areas from eed ated integrated (Advanced Trailes) / 64 byte cases data 4 times process.	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size /	Stop Grar ftware exe 8-way set ress bus t	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers	ons 2 (144 newstep™ technology data areas from eed ated integrated (Advanced Trailes) / 64 byte cases data 4 times process.	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size /	Stop Grar ftware exe 8-way set ress bus t	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Trailes) / 64 byte cas data 4 times publity / 36-bit ad	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus tress bus is	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Tranes) / 64 byte cas data 4 times point units; 1 lo	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus to	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Dut-of-order instructions	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Tranes) / 64 byte cas data 4 times point units; 1 loion execution)	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus to	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Dut-of-order instructions Branch prediction	Streaming SIMD Extensis Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Tranes) / 64 byte cas data 4 times point units; 1 loion execution)	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus to	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Out-of-order instructions Branch prediction Speculative execution	Streaming SIMD Extensic Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 loion execution) ary) Execution)	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus to	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Dut-of-order instructions Branch prediction Speculative execution Math coprocessor	Streaming SIMD Extensis Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 loion execution) ary) Execution) nit	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / interclock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus to	new instruction, Deep Sleed cution associative cransfers at 2	ep, Deeper / integrated 2 times per 0	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path L3 cache System bus Memory addressability System bus - width Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility	Streaming SIMD Extensis Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 bytensions) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic Pipelined floating point u Compatible with IA-32 so	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 loion execution) ary) Execution) nit oftware	instructions) ingy, Auto Halt, m malicious so insfer Cache) che line size / iner clock) / add dressing / addi	Stop Grar ftware exe 8-way set ress bus t ress bus is	nt, Deep Sleecution associative ransfers at 3	ons) ep, Deeper / integrated 2 times per c	/ unified (inte	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path L3 cache System bus Memory addressability System bus - width Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility Technology (micron)	Streaming SIMD Extensisenhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 byte) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic Pipelined floating point un Compatible with IA-32 so 0.09 micron or 90 nanomemore	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 lo ion execution) ary) Execution) nit oftware	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / inser clock) / add dressing / additionad unit; 1 store	Stop Grar ftware exe 8-way set ress bus is e unit	associative as double clo	/ integrated 2 times per ccked at 200	/ unified (inte clock / 64 byte MHz	rnal die; on die)
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility	Streaming SIMD Extensis Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 bytension) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic Pipelined floating point un Compatible with IA-32 so 0.09 micron or 90 nanom Micro Flip-Chip Pin Grie	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 lo ion execution) by yory) Execution) nit oftware neter (705, 705 and Array (Micro	instructions) ingy, Auto Halt, in malicious so insfer Cache) che line size / inser clock) / add dressing / additionad unit; 1 store inser clock) inser clock) / add dressing / additionad unit; 1 store inser clock) / add inserting / additional clock	Stop Grar ftware exe 8-way set ress bus is e unit	associative as double cloopin surface	/ integrated 2 times per ccked at 200N	/ unified (inte	rnal die; on die) e cache line size
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Dut-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility Fechnology (micron) Package and connector	Streaming SIMD Extensisenhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 bytension) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic Pipelined floating point un Compatible with IA-32 so 0.09 micron or 90 nanom Micro Flip-Chip Pin Grie (mPGA479M socket) or	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Transes) / 64 byte cases data 4 times point units; 1 loion execution) bry) Execution) bry Execution) fitware neter (705, 705a d Array (Micro	instructions) agy, Auto Halt, m malicious so asfer Cache) che line size / per clock) / add dressing / add addressing / addressing / add addressing /	Stop Grar ftware exe 8-way set ress bus is e unit	associative as double cloopin surface	/ integrated 2 times per ccked at 200N	/ unified (inte	rnal die; on die) e cache line size
Power mgmt technology Hyper-Threading Execute Disable Bit Intel 64 Technology 1 cache - bus 1 data cache 1 instruction cache 2 cache - size 2 cache - data path 3 cache System bus Memory addressability System bus - width Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility Fechnology (micron)	Streaming SIMD Extensis Enhanced Intel SpeedS No Some: protects memory None 256-bit data path / full sp 32KB data cache / integr 32KB instruction cache / 1MB or 2MB / full speed 256-bit data path (32 bytension) None 400 or 533MHz (transfers 64GB memory addressal 64-bit data path 2 integer units; 1 floating Yes (out-of-order instruct Dynamic (based on histo Yes (Advanced Dynamic Pipelined floating point un Compatible with IA-32 so 0.09 micron or 90 nanom Micro Flip-Chip Pin Grie	ons 2 (144 new step™ technolo data areas from eed ated integrated (Advanced Trailes) / 64 byte cases data 4 times point units; 1 loion execution) bry) Execution) bry Execution) of the enter (705, 705 and Array (Micro Micro Flip-Ch Express Chips	instructions) agy, Auto Halt, m malicious so asfer Cache) che line size / per clock) / add dressing / add addressing / addressing / add addressing /	Stop Grar ftware exe 8-way set ress bus is e unit	associative as double cloopin surface	/ integrated 2 times per ccked at 200N	/ unified (inte	rnal die; on die) e cache line size

Intel® Pentium® III Xeon ^{TI}		
Codename	Tanner	Cascades
Positioning	Mid-range and higher servers and workstations	Same
Instruction architecture	CISC/RISC/micro-ops	Same
MMX™ / Streaming SIMD	MMX / Streaming SIMD Extensions (SIMD)	Same
_1 cache - bus	64-bit / full speed	Same
_1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking	Same
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	Same
L1 cache - organization	4-way set associative (data); 2-way set associative (instruction)	Same
L1 cache - parity	Parity in cache and internal registers	Same
L2 cache - size / speed	512KB, 1MB, or 2MB / full speed	256KB / full speed (Advanced Transfer Cache)
L2 cache - data path	64-bit path / ECC	256-bit data path / quad-wide cache line / ECC
L2 cache - buffering	None	Intelligent buffering of read and stores (called
		Advanced System Buffering with 4 writeback
		buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	4 way set associative	8-way set associative
L2 cache - write policy	Write-through or write-back (programmable per line),	Same
	uncacheable, write-protect	
L2 cache - controller	Integrated / unified L2 cache (external die) / CSRAM	Integrated controller / unified (internal die; on die)
L2 cache - type	Non-blocking / pipelined burst synchronous	Same
System bus - speed	100MHz	133MHz
System bus - width	64-bit system bus with ECC	Same
System address bus	36-bits (4GB memory cacheability; 64GB memory addressability) /	Same
System hus parity	PSE-36 / Intel Extended Server Memory Architecture (PSE-36)	Sama
System bus - parity Execution units	ECC on system bus; parity on address bus (frontside bus)	Same Same
	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit Decoupled, 14 stage superpipelined	Same
Pipeline stages Supscal dispatch/ovecute	5 micro-ops per cycle (3 micro-ops is typical)	Same
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	Same
Superscalar retire	3 micro-ops per cycle	Same
•	Yes (called dynamic execution)	Same
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically	Same
Branomprediction	predicts 10 to 15 nested branches	Carrio
Speculative execution	Yes (typically 20 to 30 instructions beyond counter; 5 average)	Same
Math coprocessor	Pipelined math coprocessor	Same
Voltage regulation	External Voltage Regulation Module (VRM)	On-Cartridge Voltage Regulation
Serial number	Unique processor serial number (software-accessible)	Same
Bus architecture	Independent backside and frontside buses operate	Same
	concurrently / Dual Independent Bus Architecture (DIB)	
Internal processing	32-bits (300 bit internal bus width)	Same
Word size	32-bits	Same
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD,	Same
Cache line size	40 more GPR via register renaming	Same
Burst mode bus	32 bytes (8 bytes x 4 chunks) Addr-data-data-data-data	Same
Systems management	SMBus for thermal sensor, PIROM, Scratch EEPROM	Same
Multiple processors	1-, 2-, 4-, and 8-way SMP support	1- and 2-way SMP support
Technology (micron)	0.25u or 0.18u	0.18u
Transistors	~7.5 million	~28.1 million
Package type	Single Edge Contact Cartridge (SECC)	Same
. achago typo	requires Intel Slot 2 (SC330)	Carro
	4.992 inches high x 6.000 inches wide x 0.733 inches	
Available date	April 1999 (500 and 550MHz/512KB),	October 1999 (600, 667, 733MHz),
.	September 1999 (550MHz/1 and 2MB),	January 2000 (800MHz), March 2000 (866MHz)
	May 2000 (700MHz/1 and 2MB), March 2001 (900MHz/2MB)	August 2000 (1GHz)
Frequency (MHz)	500/100MHz with 512KB L2 cache	600/133MHz with 256KB L2 cache
,	500/100MHz with 1MB L2 cache	667/133MHz with 256KB L2 cache
	500/100MHz with 2MB L2 cache	733/133MHz with 256KB L2 cache
	550/100MHz with 512KB L2 cache	800/133MHz with 256KB L2 cache
	550/100MHz with 1MB L2 cache	866/133MHz with 256KB L2 cache
	550/100MHz with 2MB L2 cache	1GHz/133MHz with 256KB L2 cache
	700/100MHz with 1MB L2 cache	
	700/100MHz with 2MB L2 cache	
	900/100MHz with 2MB L2 cache (uses same Advanced	450NX (servers), 440GX (workstations), 840
	Transfer Cache of Cascades of 256-bit L2 data path with	
Chipset support	Advanced System Buffering) 450NX (servers), 440GX (workstations), or Profusion™	
CONTRACTORIUM	TOURN (SELVELS), THUGA (WULKSLALIULIS), OF PROTUSION'"	
	perty of their respective owners	(11INTEL) Compiled by Roger Dodson, IBM, April 20

Intel® Pentium® 4 for high	h performance desktop systems
	1.3GHz, 1.4GHz, 1.5GHz, 1.6GHz, 1.7GHz, 1.8GHz, 1.9GHz
Code name Micro-architecture MMX™/Streaming SIMD SSE2	Willamette IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path	256KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Front Side Bus Memory addressability Front Side Bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Cache line size Multiple processors	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data No SMP support
Technology (micron) Transistors Package and connector	 0.18u ~42 million with die size of 217 square millimeters 1. Pin Grid Array (PGA) requires 423-pin Zero Insertion Force (ZIF) socket named Intel Socket 423 (PGA423); used with RDRAM-based 850 chipset 2. Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)
Frequency (MHz) and available date	1.3GHz: 423-pin available January 2001 1.4GHz: 423-pin available November 2000 1.5GHz: 423-pin available November 2000, 478-pin available August 2001 1.6GHz: 423-pin available November 2000, 478-pin available August 2001 1.7GHz: 423-pin available November 2000, 478-pin available August 2001 1.8GHz: 423-pin available November 2000, 478-pin available August 2001 1.9GHz: 423-pin available November 2000, 478-pin available August 2001 2.0GHz: 423-pin available November 2000, 478-pin available August 2001
Chipset support	Intel 850 with dual channel RDRAM memory Intel 845 with SDRAM memory

Code name Micro-architecture MMX™ / Streaming SIMD SSE2 Hyper-Threading	Northwood IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) 3.06GHz with 533MHz and all 800MHz system bus processors: Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path L3 cache	512KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC None
System bus	400 or 533 or 800MHz (transfers data four times per clock) / address bus transfers at two times per clock /
Memory addressability Frontside bus - width	64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Multiple processors	Compatible with IA-32 software No SMP support
Technology (micron) Transistors Package and connector	0.13u ~55 million Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket
Frequency and available date	1.6GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 2.0GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 2.0GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8A GHz with 400MHz system bus: available July 2002 2.0A GHz with 400MHz system bus: available January 2002 ("A" signifies the 0.13 micron version, not 0.18 micron) 2.2GHz with 400MHz system bus: available May 2002 2.4GHz with 533MHz system bus: available May 2002 2.4G GHz with 800MHz system bus: available May 2002 2.5GHz with 400MHz system bus: available May 2002 2.5GHz with 533MHz system bus: available May 2002 2.6G GHz with 800MHz system bus: available May 2002 2.6G GHz with 400MHz system bus: available May 2002 2.6G GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.6G GHz with 800MHz system bus: available August 2002 2.6G GHz with 400MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 800MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 400MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 533MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available August 2002 2.6G GHz with 633MHz system bus: available Augu
Chipset support	Intel 850 or 850E with dual channel RDRAM memory Intel 845 with SDRAM or DDR-SDRAM memory Intel 865 family with single or dual channel DDR-SDRAM memory (400, 533, or 800 MHz system bus) Intel 875P with single or dual channel DDR-SDRAM memory (800 MHz system bus)

Intel® Pentium® 4 for des	ktop systems	
Code name Micro-architecture MMX™ / Streaming SIMD SSE2 SSE3 Hyper-Threading	Prescott IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipe MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) Streaming SIMD Extensions 3 (13 new instructions) 800MHz system bus processors: Hyper-Threading (HT) Technology (har	uctions)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 16KB data cache / 4-way set associative / write-through / 64 byte cache li Size not published / holds 12,000 micro-ops / 8-way set associative / integ called Execution Trace Cache; caches decoded x86 instructions (micro-o	grated /
L2 cache - size L2 cache - data path L3 cache	1MB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache sectors) / 8-way set associative / integrated / unified (internal die; on die). None	
System bus Memory addressability System bus - width	533 or 800MHz (transfers data four times per clock) / address bus transfe 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double of 64-bit data path	·
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequer Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers	ncy (Rapid Execution Engine)
Compatibility Multiple processors Other features	Compatible with IA-32 software No SMP support Thermal monitoring, built-in self test, IEEE 1149.1 standard test access po	ort and boundary scan
Technology Package and connector	90nm (nanometer) or 0.09u (micron) Flip-Chip Pin Grid Array (FC-mPGA4) requires 478-pin surface moun named mPGA478B socket	nt Zero Insertion Force (ZIF) socket
Frequency and available date	2.80A GHz with 533MHz system bus 2.80E GHz with 800MHz system bus with Hyper-Threading Technology 3.00E GHz with 800MHz system bus with Hyper-Threading Technology 3.20E GHz with 800MHz system bus with Hyper-Threading Technology 3.40E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004 available February 2004 available February 2004 available February 2004 available February 2004
Chipsetsupport	Intel 865 family with single or dual channel DDR-SDRAM memory Intel 875P with single or dual channel DDR-SDRAM memory	

[Desktop] Intel Pentium 4 Processor 5xx

Intel® Pentium® 4 for des	sktop systems	Clock	L2 cache	System	Disable	Threading	Enhanced Intel	_64	Available	
Intel Deutium 4 December	* 505	speed					y Technology	Tech		
Intel Pentium 4 Processo Intel Pentium 4 Processo		2.66GHz 2.66GHz				No No	No No	No No	Jul 05	
Intel Pentium 4 Processo		2.66GHz				No No	No No	No Yes	Jul 05 Jul 05	
Intel Pentium 4 Processo		2.93GHz				No	No	No	Nov 04	
Intel Pentium 4 Processo		2.93GHz				No	No		Jun 05	
Intel Pentium 4 Processo		3.06GHz				No	No	No	Jul 05	
Intel Pentium 4 Processo		3.06GHz				No	No	Yes	Jul 05	
	r supporting Hyper-Threading Technology 520			800MHz		HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 520J			800MHz		HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 521			800MHz		HT	No		May 05	
	r supporting Hyper-Threading Technology 524	3.06GHz				HT	No	Yes	July 06	
	r supporting Hyper-Threading Technology 530	3.0GHz	1MB	800MHz	No	HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 530J	3.0GHz	1MB	800MHz	Yes	HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 531	3.0GHz	1MB	800MHz	Yes	HT	No	Yes	May 05	
	r supporting Hyper-Threading Technology 540	3.2GHz	1MB	800MHz	No	HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 540J	3.2GHz	1MB	800MHz	Yes	HT	No	No	Jun 04	
Intel Pentium 4 Processo	r supporting Hyper-Threading Technology 541	3.2GHz	1MB	800MHz	Yes	HT	No	Yes	May 05	
Intel Pentium 4 Processo	r supporting Hyper-Threading Technology 550	3.4GHz	1MB	800MHz	No	HT	No	No	Jun 04	
Intel Pentium 4 Processo	r supporting Hyper-Threading Technology 550J	3.4GHz	1MB	800MHz	Yes	HT	No	No	Jun 04	
	r supporting Hyper-Threading Technology 551	3.4GHz	1MB	800MHz	Yes	HT	No	Yes	May 05	
	r supporting Hyper-Threading Technology 560	3.6GHz	1MB	800MHz	No	HT	No	No	Jun 04	
Intel Pentium 4 Processo	r supporting Hyper-Threading Technology 560J	3.6GHz	1MB	800MHz	Yes	HT	No	No	Jun 04	
Intel Pentium 4 Processo	r supporting Hyper-Threading Technology 561	3.6GHz	1MB	800MHz	Yes	HT	No	Yes	May 05	
	r supporting Hyper-Threading Technology 570J	3.8GHz	1MB	800MHz	Yes	HT	No	No	Nov 04	
	r supporting Hyper-Threading Technology 571	3.8GHz	1MB	800MHz	Yes	HT	No	Yes	May 05	
SSE3 Hyper-Threading Execute Disable Bit Intel 64 Technology¹ L1 cache - bus L1 data cache L1 instruction cache L2 cache - size L2 cache - data path	Streaming SIMD Extensions 3 (13 new instructions Some: Hyper-Threading (HT) Technology (hard Some: protects memory data areas from malicins Some: Intel 64 Technology 256-bit data path / full speed 16KB data cache / 4-way set associative / write-Size not published / holds 12,000 micro-ops / 8-called Execution Trace Cache; caches decoded 1MB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each sectors) / 8-way set associative / integrated / un	-through / 6 -way set as x86 instructions	64 byte sociatetions	e cache lii ive / integ (micro-op	ne / inte rated / s)	grated		vo 64	byte	
L3 cache	None	o ols) / o ddr	b.	ua transfai	o ot tur	times no	r alaak /			
System bus Memory addressability	533 or 800MHz (transfers data four times per clife64 byte cache line size64GB memory addressability / 36-bit addressing	,				·				
System bus - width	64-bit data path						-, -: -: -: -: -: -: -: -: -: -: -: -: -:			
Execution units	2 integer units; 1 floating point units; 1 load unit; Two integer units (or Arithmetic Logic Units) run			e frequen	cy (Rap	id Execut	ion Engine)			
Out-of-order instructions	Yes			-	•		- '			
Branch prediction	Dynamic (based on history) / 4KB Branch Targe	et Buffer								
Speculative execution	Yes (Advanced Dynamic Execution)									
Math coprocessor	Pipelined floating point unit / handles 128-bit flo	ating point	regist	ers						
Compatibility Other features	Compatible with IA-32 software (some compatible Thermal monitoring, built-in self test, IEEE 1149			,	ort and	boundary	scan			
Technology Package and socket										
Chipset support	Intel 915G, 915GV, 915P, 925X, and 925XE Exp	oress chips	et or o	other com	patible (chipsets				

[Desktop] Intel Pentium 4 Processor 6xx

	Intel® Pentium® 4 supporting Hyper-Threading Technology												
for desktop systems		Clock speed	L2 cache	Core	System bus	Intel Virtualization Technology	Execute Disable Bit	Threading	Enhanced Inte SpeedStep™ Technology	l Intel 64 Tech	Process	Available date	
Intel Pentium 4 Processor	r 620	2.80GHz	2MB	Single	800MHz	: No	XD	HT	EIST	EM64T	90nm	Aug 2006	
Intel Pentium 4 Processor	r 630	3.00GHz	2MB	Single	800MHz	: No	XD	HT	EIST	EM64T	90nm	Feb 2005	
Intel Pentium 4 Processor	r 631	3.00GHz	2MB	Single	800MHz	: No	XD	HT	EIST	EM64T	65nm	Jan 2006	
Intel Pentium 4 Processor	r 640	3.20GHz	2MB	Single	800MHz	: No	XD	HT	EIST	EM64T		Feb 2005	
Intel Pentium 4 Processor		3.20GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T		Jan 2006	
Intel Pentium 4 Processor		3.40GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T		Feb 2005	
Intel Pentium 4 Processor		3.40GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T		Jan 2006	
Intel Pentium 4 Processor		3.60GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T		Feb 2005	
Intel Pentium 4 Processor		3.60GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T		Jan 2006	
Intel Pentium 4 Processor		· · · · · · · · · · · · · · · · · · ·											
Intel Pentium 4 Processor Intel Pentium 4 Processor		3.80GHz	2MB	Single	800MHz		XD	HT	EIST	EM64T	90nm	Nov 2005	
Code name Core Micro-architecture MMX [™] / Streaming SIMD SSE2	Single IA-32 MMX ^{TI} Stream	/ NetBurst [⊤] M (57 new i ming SIMD	M (CISC nstruction Extensi	/RISC/mi ons) / Str ons 2 (14	icro-ops) eaming S 14 new ins	structions)				1			
Hyper-Threading Execute Disable (XD) Bit Intel 64 Technology ¹	Enhan Hyper Protect Intel 6	eaming SIMD Extensions 3 (13 new instructions) hanced Intel SpeedStep™ Technology per-Threading (HT) Technology (hardware support for multi-threaded applications) otects memory data areas from malicious software execution el 64 Technology me: Intel Virtualization Technology											
L1 cache - bus L1 data cache L1 instruction cache	16KB Size n	ot publishe	d / 4-way d / hold	/ set asso s 12,000	micro-op:	write-through s / 8-way set a oded x86 instr	associativ	/e / integrate	•				
L2 cache - size L2 cache - data path L3 cache	256-bi		(32 byt	es) / tran	sfers on e	e) each bus clock I / unified (inte				y divided	I into two	64 byte	
System bus		•		our times	s per clocl	k) / address b	us transfe	ers at two tir	nes per clock	/			
Memory addressability System bus - width	64GB	e cache lin memory ad data path		bility / 36	-bit addre	essing / addre	ss bus is	double clocl	ked at 200, 26	66, or 40	0MHz		
Execution units			U	•	-	unit; 1 store (frequency (Rapid Execut	tion Engi	ne)		
Out-of-order instructions Branch prediction Speculative execution Math coprocessor	Yes (A	dvanced D	ynamic	Éxecutio	n)	Target Buffer	nt registe	rs					
Compatibility Other features		atible with nal monitori				e 1149.1 standa	ard test a	ccess port a	and boundary	scan			
Process technology Package and socket	, , , , , , , , , , , , , , , , , , , ,												
Chipset support	Intel 9	15 chipset	family, 9	925X, 925	5XE, 945	chipset family	, 955X, o	r other com	patible chipse	ets			

[Desktop] Intel Pentium D Processor 8xx

Intel® Pentium® Process	or D Proces	ssor										
for desktop systems	Clock speed	L2 cache	System bus	Package	Core	Hyper- Threading Technology	Total threads (logical)	Virtualization Technology		Enhanced Inte SpeedStep™ Technology	l Intel 64 Tech	Available date
Pentium D Processor 820 Pentium D Processor 830 Pentium D Processor 840	3.00GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2 2 2	No No No	Yes Yes Yes	No Yes Yes	EM64T EM64T EM64T	Jun 05 Jun 05 Jun 05
- T CHILITH D 1 10003301 040	3.20 0 112	ZXTIVID	OOOIVII IZ	TO LOA4	Duai	NO	2	140	103	103	LIVIOTI	Jun 03
Processor generation Core Formal name Micro-architecture MMX TM / Streaming SIMD SSE2 SSE3 Power mgmt technology Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology¹ Virtualization Technology	MMX TM (57 Streaming Streaming Some: Enh No Two thread Protects me Intel 64 Tec 64 bit exter	Burst™ ((new inst SIMD Ex SIMD Ex nanced Ir s (two co emory da chnology	CISC/RISC ructions) / tensions 2 tensions 3 ntel Speed res with nata areas ((an exten	/ Streaming 2 (144 new 3 (13 new i 4Step™ Tec no Hyper-T from malici sion to the	g SIMI instructionstructions chnolochread ous so IA-32	D Extension cuctions) ections) egy eing support oftware exe	provide to	two logical pr	s)			
L1 cache - bus L1 data cache L1 instruction cache		data cacl ıblished /	nes / 4-wa two instru	uction cach	es (ea	ach hold 12	,000 micı			grated sociative / inte	grated /	
L2 cache - size L2 cache - data path L3 cache		a path (3	2 bytes) /	transfers o	n eac	h bus clock	/ 128 by	,	,	ally divided in	to two 64	1 byte
System bus	800MHz (tr 64 byte cad			imes per cl	lock) /	address bu	ıs transfe	ers at two time	es per clo	ock /		
Memory addressability Frontside bus - width	64GB mem 64-bit data	•	essability	/ 36-bit ad	dressi	ing / addres	s bus is	double clocke	ed at 200,	, 266, or 400M	lHz	
Execution units	2 integer un Two integer		٠.					frequency (R	apid Exe	cution Engine))	
Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility	Yes Dynamic (by Yes (Advantage) Pipelined floor Compatible	ced Dynoating po	amic Exec oint unit / I	cution) nandles 12	8-bit f	-	ıt register	rs				
Technology (micron) Package and connector	90nm or 0.0 775-land F		Land Gri	d Array (F	C-LG	A4) packaç	ge requir	es LGA775	socket (s	socket also cal	led Sock	et T)
Chipset support	Intel 945 E	xpress ch	nipset fam	ily, 955X E	xpres	s chipset						

[Desktop] Intel Pentium D Processor 9xx

Intel® Pentium® Processor D Processor

inter Pentium Process	or D Proces	SOF									1.4.1			
for desktop systems	Clock	L2	System		Hyper- Threading	Total threads	Virtualization		Enhanced Intel SpeedStep™	Intel 64	Intel Viiv™	Available		
	speed	cache	bus	Core	Technology	(logical)	Technology	Bit	Technology	Tech	Tech	date		
Pentium D Processor 915	2 800 47	2v2MB	900MH-			2	No	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 920						2	Yes	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 925						2	No	Yes	Yes	EM64T	Viiv	Oct 06		
Pentium D Processor 930						2	Yes	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 935						2	No	Yes	Yes	EM64T	Viiv	Jan 07		
Pentium D Processor 940	3.20GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 945	3.40GHz	2x2MB	800MHz	Dual	No	2	No	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 950	3.40GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06		
Pentium D Processor 960	3.60GHz	3.60GHz 2x2MB 800MHz Dual No 2 Yes Yes Yes EM64T Viiv May 0												
												•		
Processor generation	Presler													
Core	Dual-core													
Formal name	Intel Penti	um D Pr	ocessor											
Micro-architecture				C/mic	ro-ons) / 20	stage nir	neline (Hyner	-nineline	d technology)					
MMX™ / Streaming SIMD														
SSE2							ons (70 new i	i isti uctio	1115)					
	Streaming													
SSE3	Streaming					lions)								
Power mgmt technology		nanced Intel SpeedStep™ Technology												
Hyper-Threading	No	o threads (two cores with no Hyper-Threading support provide two logical processors)												
Total threads	Two thread	s (two co	ores with n	ю Нур	er-Threadii	ng suppo	rt provide two	logical _l	processors)					
Execute Disable (XD) Bit	Protects me	emory da	ata areas t	from r	nalicious so	ftware ex	recution							
Intel 64 Technology ¹	Intel 64 Tec	hnology	(an exten	sion to	the IA-32	instructio	n set which a	ıdds						
	64 bit exter	ntel 64 Technology (an extension to the IA-32 instruction set which adds 4 bit extensions to the x86 architecture)												
Virtualization Technology														
Viiv Technology	Intel Viiv Te				9)									
		or in lolog,	,											
L1 cache - bus	256-bit data	a nath / f	ull speed											
L1 data cache		•	•	w cot	accociativo	/ write th	rough / 64 by	to cacho	line / integrate	٨				
											watad /			
L1 instruction cache									way set associa	itive / integ	grated /			
	called Exec	cution ira	ice Cacne	; cacr	ies aecoae	x86 insi	tructions (mic	ro-ops)						
LO sasha sisa	T OMD /			/ 611			(0)							
L2 cache - size							ansfer Cache							
L2 cache - data path	256-bit data	a path (3	2 bytes) /	transf	ers on each	bus cloc	k / 128 byte (cache lin	e size (usually	divided int	o two 6	4 byte		
	sectors) / 8	-way set	associativ	ve / in	tegrated / u	nified (int	ernal die; on	die) / EC	C					
L3 cache	None													
System bus	800MHz (tr	ansfers o	data four t	imes į	per clock) /	address I	bus transfers	at two tir	mes per clock /					
•	64 byte cac	che line s	size		,				•					
Memory addressability	,			/ 36-h	oit addressir	ng / addre	ess bus is dou	ıble cloc	ked at 200, 266	or 400M	Hz			
Frontside bus - width	64-bit data	•	000000	, 00 2		.9 /				, 000				
Trontside bas Width	O+ Dit data	patii												
Execution units	2 integer ur	nite: 1 fla	ating noin	t unite	: 1 load uni	t· 1 store	unit							
Excounter units								auono:	Panid Evacution	n Enginal				
Out of order instructions		units (0	HIIIIII	IC LOC	jie oriits) ru	ıı aı IWO I	intes core ite	quency ((Rapid Execution	ııı ⊑ııgırıe)				
Out-of-order instructions														
Branch prediction	,		,		Branch Targ	et Buffer								
Speculative execution	Yes (Advan	iced Dyn	amic Exec	cution)									
Math coprocessor	Pipelined fl	oating po	oint unit / I	nandle	es 128-bit flo	oating po	int registers							
Compatibility	Compatible	with IA-	32 and EN	И64T	software									
Process technology	65nm or 0.0	065u												
Package and connector	775-land F	lip-Chip	Land Gri	d Arr	ay (FC-LGA	A6) pack	age requires	LGA77	5 socket (socke	et also cal	led Soci	ket T)		
					- ,	<i>,</i> .	<u> </u>		,					
Chipset support	Intel 945 Ex	xpress cl	hipset fam	ilv. 95	5X and 975	X Expres	ss chipset							
h 1 1	0 .0/	,	r	.,,										

Intel® Pentium® 4 Proces		tion						vecute	Hyner-	Enhanced Into	al	
for high-end gamers and	i power users	Clock speed	L2 cache	L3 cache	System bus	Core		Disable	Threading	J SpeedStep™ V Technology	1	Available date
Intel Pentium 4 Processor Intel Pentium 4 Processor Intel Pentium 4 Processor Intel Pentium 4 Processor Intel Pentium 4 Processor	r Extreme Edition r Extreme Edition r Extreme Edition	3.4GHz 3.4GHz 3.46GHz	512KB 512KB	2MB 2MB 2MB	800MHz 800MHz 800MHz 1066MHz 1066MHz	Single Single Single		No No No	HT HT HT HT	No No No No No	No No No No Yes	Nov 03 Feb 04 Jun 04 Nov 04 Feb 05
Code name Core Formal name Micro-architecture MMX™/Streaming SIMD SSE2 SSE3 Power mgmt technology Hyper-Threading Execute Disable (XD) Bit EM64T	Streaming SIMD 3.73GHz only: S None Hyper-Threading	Processor (CISC/RI nstructions Extension treaming S (HT) Tech rotects me	with HT SC/micro s) / Strea s 2 (144 SIMD Ext anology (1 mory dat	o-ops) / ming S new ins tension hardwa ta areas	/ 20 stage p IMD Extens structions) s 3 (13 new are support f s from malic	ipeline (l sions (70 instruct for multi-	Hyper-pipe) new instru ions) threaded a	ictions) pplicat			intel inside	EXTREME H
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path 8KB data cache / Size not publishe called Execution	4-way set d / holds 1	associa 2,000 m	icro-op	s / 8-way se	t associ	ative / integ	grated /				
L2 cache - size L2 cache - data path	512KB or 2MB / 1 256-bit data path sectors) / 8-way s	(32 bytes)	/ transfe	ers on e	each bus clo	ck / 128	•		ize (usual	ly divided into) two 64 b	oyte
L3 cache		lata path (-		sfers on eac			te cach	ne line size	e / 8-way set a	associati	ve/
System bus Memory addressability Frontside bus - width	800MHz or 1066 64 byte cache lin 64GB memory ac 64-bit data path	e size			·	,				·		
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	2 integer units; 1 Two integer units Yes Dynamic (based Yes (Advanced Desiration of the control	on history)	etic Log / 4KB B kecution)	ic Units ranch T)	run at two	times co er		ncy (Ra	pid Execu	ition Engine)		
Compatibility Multiple processors	Compatible with I No SMP support	A-32 softw	/are (son	ne com	patible with	EM64T	software)					
Technology (micron) Package and connector	0.13u (3.73GHz i	id Array-2	(FC-PG	iA2) re	quires 478	pin sur	face mour	ıt Zero	Insertion	Force (ZIF)	socket	

775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket (socket also called Socket T)

named mPGA478B socket or

Intel 848P, 865 family, and 875P for FC-PGA2 package

Intel 925XE Express supports 1066MHz system bus

Intel 915G, 915P, 925X, and 925XE Express chipset for FC-LGA4 package

Chipset support

		Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Ti	hreading Technology	Available date
Mobile Intel Pentium 4 Pro Mobile Intel Pentium 4 Pro Mobile Intel Pentium 4 Pro Mobile Intel Pentium 4 Pro Mobile Intel Pentium 4 Pro	ocessor 532 ocessor 538 ocessor 548	2.8GHz 3.06GHz 3.2GHz 3.33GHz 3.46GHz	1MB 1MB 1MB 1MB 1MB	No No No No No	533MHz 533MHz 533MHz 533MHz 533MHz	Hyper-Th Hyper-Th Hyper-Th	nreading Technology nreading Technology nreading Technology nreading Technology nreading Technology	June 2004 June 2004 June 2004 September 2004 January 2005
Messaging Micro-architecture MMX™ / Streaming SIMD SSE2 SSE3 Hyper-Threading Power mgmt technology Execute Disable Bit	replacemen IA-32 / NetE MMX™ (57 Streaming S Streaming S Hyper-Threa	ts" typically fe Burst™ (CISC/ new instructio SIMD Extensic SIMD Extensic ading (HT) Tec	aturing lar RISC/micr ns) / Strea ons 2 (144 ons 3 (13 r chnology (ge screens, ro-ops) / 20 s aming SIMD new instruction hew instruction	full-size keybo stage pipeline (Extensions (70 tions) ons) pport for multi-	ards, and (Hyper-pip) new inst -threaded	·	known as "desktop
_1 cache - bus _1 data cache _1 instruction cache	16KB data of Size not pub	olished / holds	set associ 12,000 m	nicro-ops / 8-	through / 64 b way set assoc x86 instruction	iative / inte		
L2 cache - size L2 cache - data path L2 cache - data path L3 cache L3 cache L3 cache L3 cache L3 cache L5 cache L6 cache - size L6 cache - data path L7 full speed (Advanced Transfer Cache) L8 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC None								
System bus Memory addressability System bus - width		ory addressab					two times per clock / 6 e clocked at 266MHz	4 byte cache line size
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	Two integer Yes (out-of-operation of Dynamic (bayes) Yes (Advance)	order instruction ased on histor ced Dynamic I	metic Log on executi y) / 4KB E Execution)	ic Units) run on) Branch Targe	at two times c		ency (Rapid Executior	n Engine)
Compatibility Multiple processors Other features	No SMP su			t, IEEE 1149	.1 standard te	st access	port and boundary sc	an
Process technology Package and connector	Flip-Chip P	meter) or 0.09 in Grid Array '8-pin surface	(FC-mPG	A4) packag		socket (r	mPGA478B socket)	
Frequency	2.8GHz 3.06GHz 3.2GHz 3.33GHz 3.46GHz		3.06 3.20 3.33	GHz, 88 watt GGHz, 88 wa GHz, 88 watt GGHz, 88 wa	nance Mode is at 1.25-1.40 tts at 1.25-1.4 is at 1.25-1.40 tts at 1.25-1.4 tts at 1.25-1.4	0 volts volts 0 volts	Battery Mode 1.86GHz, 1.15 volts	
Chipset support		ME, 852PM choatible chipse	-					

Intel® Pentium® Processor Extreme Edition for high-end gamers and power users	On Clock speed	L2 cache	System bus	Package	Core	Hyper- Threading Technology	threads	Disable	Enhanced Inte SpeedStep™ Technology	64	Available date
Pentium Processor Extreme Edition 840	3.20GHz	2x1MB	800MHz	FC-LGA4	Dual	Yes	4	Yes	No	EM64T	Apr 05

Processor generation Smithfield Core Daul core Formal name **Intel Pentium Processor Extreme Edition** Micro-architecture IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ / Streaming SIMD MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) SSE₂ Streaming SIMD Extensions 2 (144 new instructions) SSE3 Streaming SIMD Extensions 3 (13 new instructions) Power mgmt technology None Hyper-Threading Hyper-Threading (HT) Technology (hardware support for multi-threaded applications) Total threads Four threads (two cores each supporting Hyper-Threading provides four logical processors) Execute Disable (XD) Bit Protects memory data areas from malicious software execution Intel 64 Technology¹ Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture) L1 cache - bus 256-bit data path / full speed Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated L1 data cache L1 instruction cache Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops) L2 cache - size Two 1MB (one for each core) / full speed (Advanced Transfer Cache) L2 cache - data path 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC L3 cache System bus 800MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size Memory addressability 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz Frontside bus - width 64-bit data path **Execution units** 2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Out-of-order instructions Dynamic (based on history) / 4KB Branch Target Buffer Branch prediction Speculative execution Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers Math coprocessor Compatibility Compatible with IA-32 and EM64T software Technology (micron) 90nm or 0.09u Package and connector 775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket (socket also called Socket T) Intel 955X Express chipset Chipset support

[Desktop] Intel Pentium Processor Extreme Edition 9xx

Intel® Pentium® Processor Extreme Edition

for high-end gamers an	d power users	Clock speed	L2 cache	System bus MHz		Core	Hyper- Threading Technology	threads	ization	Execute Disable Bit	Enhanced Int SpeedStep™ Technology	M 64	Available date
Pentium Processor Extree Pentium Processor Extree								4 4	Yes Yes	Yes Yes	No No		Jan 06 Mar 06
Processor generation Core Formal name Micro-architecture MMX™ / Streaming SIMD SSE2 SSE3 Power mgmt technology Hyper-Threading Total threads Execute Disable (XD) Bit Intel 64 Technology¹	Streaming SIM Streaming SIM None Hyper-Threadi Four threads (1 Protects memorished 64 Technology) which adds 64	st™ (CISC. w instruction ID Extensi ID Extensi ID Extensi ID (HT) Te two cores or ory data ar blogy (an e bit extens	/RISC/mons) / Stons 2 (1 ons 3 (1 echnologeach sureas from extension to to sons)	nicro-o reamir 44 new 3 new gy (hard pportin n malid n to the	ps) / 20 sta gg SIMD Ex w instruction instruction dware supp gg Hyper-Ti cious softwa e IA-32 inst	etensions) s) oort for reading are exeruction	ons (70 nev r multi-threang provides ecution	w instruc	tions) plication	ns)			
L1 cache - bus L1 data cache L1 instruction cache	256-bit data pa Two 16KB data Size not publis called Execution	ath / full sp a caches / hed / two i	eed 4-way s	on cac	hes (each l	nold 1	2,000 micro	o-ops)/	8-way s			rated /	
L2 cache - size L2 cache - data path L3 cache	Two 2MB (one 256-bit data pa sectors) / 8-wa None	ath (32 byte	es) / trai	nsfers	on each bu	s cloc	k / 128 byte	e cache		e (usually	y divided into	two 64	byte
System bus Memory addressability Frontside bus - width	1066MHz (tran 64 byte cache 64GB memory 64-bit data pat	line size addressa		·	,					per cloc	k /		
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor Compatibility	2 integer units; Two integer un Yes Dynamic (base Yes (Advanced Pipelined floati Compatible wit	its (or Aritled on history In Dynamic Ing point u	hmetic L ry) / 4K Executi nit / han	ogic U B Bran on) dles 12	Inits) run at ch Target E 28-bit floati	two ti Buffer	imes core f	·	y (Rapi	d Execut	ion Engine)		
Process technology Package and connector	65nm or 0.065 775-land Flip-		d Grid A	Array (FC-LGA6)	packa	age require	es LGA7	775 soc	cket (soc	ket also calle	ed Socke	et T)
Chipset support	Intel 975X Exp	ress chips	et										

Intel Core Solo Processor

Intel® Core™ Solo processor for mobile and desktop systems	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz		Hyper- Threading Technology	threads	ization		Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail- able date
Ultra Low Voltage (ULV)												
Intel Core Solo processor ULV U1300	1.06GHz	800MHz	2MB	533MHz	Single	e No	1	Yes	Yes	Yes	No	Apr 2006
Intel Core Solo processor ULV U1400	1.20GHz	800MHz	2MB	533MHz	Single	e No	1	Yes	Yes	Yes	No	Apr 2006
Intel Core Solo processor ULV U1500	1.33GHz	800MHz	2MB	533MHz	Single	e No	1	Yes	Yes	Yes	No	Jan 2007
Intel Core Solo processor T1300	1.66GHz	1.0GHz	2MB	667MHz	Single	e No	1	No	Yes	Yes	No	Jan 2006
Intel Core Solo processor T1400	1.83GHz	1.0GHz	2MB	667MHz	Single	e No	1	No	Yes	Yes	No	May 2006

U=<14 watts; L=15-24 watts; T=25-49 watts; E=>50 watts

Processor generation Yonah

Marketing name Intel Core Solo processor

Core Single-core

Part of the Intel Centrino™ mobile technology when included with an Intel 945 Express Chipset family and Branding

Intel PRO/Wireless Network Connection wireless chip

Micro-architecture IA-32 / micro-op fusion, Advanced Stack Management

MMX™ / Streaming SIMD MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)

SSE2 Streaming SIMD Extensions 2 (144 new instructions) SSE3 Streaming SIMD Extensions 3 (13 new instructions)

Enhanced Intel SpeedStep™ technology, Dynamic Bus Parking, Enhanced Deeper Sleep with Dynamic Cache Sizing Power mgmt technology

Thermal management Thermal management system (digital temperature sensor and thermal monitor)

Hyper-Threading

Total threads One thread (one core with no Hyper-Threading support provides one logical processor)

Execute Disable (XD) Bit Protects memory data areas from malicious software execution

Intel 64 Technology¹

Virtualization Technology Some: Intel Virtualization Technology

L1 cache - bus 256-bit data path, full speed L1 data cache 32KB data cache / integrated L1 instruction cache 32KB instruction cache / integrated

L2 cache - size 2MB / full speed / Advanced Transfer Cache

L2 cache - data path 256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)

L3 cache None

533 or 667MHz (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size System bus Memory addressability 64GB memory addressability / 36-bit addressing / address bus is double clocked at 333MHz

System bus - width 64-bit data path

2 integer units, 1 floating point units, 1 load unit, 1 store unit **Execution units**

Math coprocessor Pipelined floating point unit Compatibility Compatible with IA-32 software

Process technology 65nm or 0.065u

U1xxx: 5.0-5.5 watts; T1300: 27 watts

Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket Package and connector

(mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)

[Ultra Low Voltage offered only in Micro Flip-Chip Ball Grid Array (Micro-FCBGA)]

Chipset support Intel 945 Express Chipset family, other compatible chipsets

Intel Core Duo Processor

Intel [®] Core™ Duo processor for mobile and desktop systems	Clock Perf Mode	Clock Battery Mode	Shared L2 cache	System bus MHz	Core	Hyper- Threading Technology	threads	ization	Execute l Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail- able date
Intel Core Duo processor U2400	1.06GHz	800MHz	2MB	533MHz	Dual	No	2	Yes	Yes	Yes	No	Sep 2006
Intel Core Duo processor U2500	1.20GHz	800MHz	2MB	533MHz	Dual	No	2	Yes	Yes	Yes	No	Jun 2006
Intel Core Duo processor L2300	1.50GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor L2400	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor L2500	1.83GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Sep 2006
Intel Core Duo processor T2300	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2300E	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	No	Yes	Yes	No	May 2006
Intel Core Duo processor T2350	1.86GHz	800MHz	2MB	533MHz	Dual	No	2	No	Yes	Yes	No	Jan 2007
Intel Core Duo processor T2400	1.83GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2450	2.00GHz	800MHz	2MB	533MHz	Dual	No	2	No	Yes	Yes	No	Jun 2007
Intel Core Duo processor T2500	2.00GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2600	2.16GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2700	2.33GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jun 2006

U (Ultra Low Voltage)=<14 watts; L (Low Voltage)=15-24 watts; T (Standard Voltage)=25-49 watts; E=>50 watts

Processor generation Yonah

Marketing name Intel Core Duo processor

Core Dual-core

Branding Part of the Intel Centrino™ Duo mobile technology when included with an Intel 945 Express Chipset family and

Intel PRO/Wireless Network Connection wireless chip

Micro-architecture IA-32 / micro-op fusion, Advanced Stack Management

MMX™ / Streaming SIMD MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)

SSE2 Streaming SIMD Extensions 2 (144 new instructions)
SSE3 Streaming SIMD Extensions 3 (13 new instructions)

Power mgmt technology Enhanced Intel SpeedStep™ technology, Dynamic Bus Parking, Enhanced Deeper Sleep with Dynamic Cache Sizing

Hyper-Threading No

Total threads Two threads (two cores with no Hyper-Threading support provide two logical processors)

Execute Disable (XD) Bit Protects memory data areas from malicious software execution

Intel 64 Technology¹ No

Virtualization Technology Some: Intel Virtualization Technology

L1 cache - bus	256-bit data path, full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated

L2 cache - size
L2 cache - data path
L3 cache - dat

L3 cache None

System bus 533 or 667MHz (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size Memory addressability 64GB memory addressability / 36-bit addressing / address bus is double clocked at 333MHz

System bus - width 64-bit data path

Execution units 2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor
Compatibility 2 integer units, 1 floating point units, 1 load unit, 1 store unit
Pipelined floating point unit
Compatible with IA-32 software

Process technology 65nm or 0.065u

Power U2xxx: 9 watts; L2xxx: 15 watts; T2xxx: 31 watts

Package and connector Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket

(mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)

Chipset support Mobile Intel 945 Express Chipset family, other compatible chipsets

Intel® Xeon™ processor	for high-performance and mid-range, dual processor enabled workstations
Code name Micro-architecture MMX™/Streaming SIMD SSE2	Foster IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path	256KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache	None
System bus Memory addressability System bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Cache line size Multiple processors Systems management	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data 2-way SMP support Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron) Transistors Package type Connector Frequency (MHz) and available date	0.18u ~42 million 603-pin micro-Pin Grid Array (PGA) Zero Insertion Force (ZIF) socket with 603 pins 1.4GHz with 400MHz FSB (available May 2001) 1.5GHz with 400MHz FSB (available May 2001) 1.7GHz with 400MHz FSB (available May 2001) 2.0GHz with 400MHz FSB (available September 2001)
Chipset support	Intel 860 with dual channel RDRAM memory

Code name P	Prostonia
Micro-architecture IA MMX™ / Streaming SIMD M SSE2 S	Prestonia Dual-processing (DP) workstations A-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 data cache 8 L1 instruction cache S	256-bit data path / full speed BKB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - data path 2	512KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache N	None
Memory addressability 6	400 or 533MHz (transfers data four times per clock [100MHz x 4 = 400MHz or 133MHz x 4 = 533MHz]) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing /
	address bus is double clocked at two times clock [100MHz \times 2 = 200MHz or 133MHz \times 2 = 266MHz] 64-bit data path
	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions Y Branch prediction D Speculative execution Y	
Cache line size 1. Multiple processors 2. Systems management 4.	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data 2-way SMP support 400MHz: thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus 533MHz: supports direct access to pins of on-die thermal diode for thermal sensor device
Package type 4 5	0.13u 400MHz: 603-pin interposer micro-Pin Grid Array (INT-mPGA) 500MHz: 604-pin flip-chip micro-PGA2 (FC-mPGA2)
Frequency (GHz) 1 and available date 2 2 2 2 2 2 2 2 2 2 3	Zero Insertion Force (ZIF) socket with 603 or 604 pins 1.8GHz with 400MHz system bus (available February 2002) 2.0GHz with 400MHz system bus (available November 2002) 2.0GHz with 533MHz system bus (available November 2002) 2.2GHz with 400MHz system bus (available February 2002) 2.4GHz with 400MHz system bus (available April 2002) 2.4GHz with 533MHz system bus (available November 2002) 2.6GHz with 533MHz system bus (available September 2002) 2.66GHz with 533MHz system bus (available September 2002) 2.8GHz with 533MHz system bus (available November 2002) 2.8GHz with 533MHz system bus (available November 2002) 3.0GHz with 533MHz system bus (available March 2003) 3.06GHz with 533MHz system bus (available March 2003)
i i	ntel 860 with dual channel RDRAM memory ntel E750x (such as E7500, E7501, E7505) with dual channel DDR-SDRAM ServerWorks® Grand Champion™ 4.0 LE
Server blade support M	Most Xeon processors listed above supported in "Performance Server Blades"

Intel® Xeon™ Processor	MP for mid-tier and back-end servers with 4-way SMP support
Code name Positioning Micro-architecture MMX™ / Streaming SIMD SSE2 Hyper-Threading	Foster MP Multi-processing (MP) workstations and servers IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path	256KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache L3 cache - data path	512KB or 1MB / full speed 256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / parity / integrated / unified (internal die; on die)
System bus Memory addressability System bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Cache line size Multiple processors Systems management	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data 4-way SMP support Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron) Package type Connector Frequency (GHz) and available date	0.18u 603-pin interposer micro-Pin Grid Array (INT-mPGA) Zero Insertion Force (ZIF) socket with 603 pins 1.4GHz with 512KB L3 cache (available March 2002) 1.5GHz with 512KB L3 cache (available March 2002) 1.6GHz with 1MB L3 cache (available March 2002)
Chipsetsupport	IBM® XA-32™ ServerWorks® GC-HE
Server blade support	Xeon MP at 1.6GHz supported in "Performance Server Blades"

Intel® Xeon™ Processor	MP for mid-tier and back-end servers with 4-way or more SMP support
Code name Positioning Micro-architecture MMX™/Streaming SIMD SSE2 Hyper-Threading	Gallatin Multi-processing (MP) workstations and servers (4-way or more SMP) IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology) MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions) Hyper-Threading Technology (hardware support for multi-threaded applications)
L1 cache - bus L1 data cache L1 instruction cache	256-bit data path / full speed 8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size L2 cache - data path	512KB / full speed (Advanced Transfer Cache) 256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache L3 cache - data path	1MB or 2MB / full speed 256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / ECC / integrated / unified (internal die; on die)
System bus Memory addressability System bus - width	400MHz (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size 64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz 64-bit data path
Execution units Out-of-order instructions Branch prediction Speculative execution Math coprocessor	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine) Yes Dynamic (based on history) / 4KB Branch Target Buffer Yes (Advanced Dynamic Execution) Pipelined floating point unit / handles 128-bit floating point registers
Compatibility Cache line size Multiple processors Systems management	Compatible with IA-32 software 128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data 4-way or more SMP support Thermal monitor, Processor Information ROM (PIROM), OEM Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron) Package type Connector Frequency (GHz) and available date	0.13u 603-pin interposer micro-Pin Grid Array (INT-mPGA) Zero Insertion Force (ZIF) socket with 603 pins 1.5GHz with 1MB L3 cache (available November 2002) 1.9GHz with 1MB L3 cache (available November 2002) 2.0GHz with 2MB L3 cache (available November 2002)
Chipsetsupport	IBM® XA-32™ ServerWorks® GC-HE

Intel® Itanium® for 64-bit	demanding enterprise and computing applications
	733MHz, 800MHz
Code name Architecture MMX™ / SIMD	Merced IA-64 (Intel Architecture 64-bit) / Explicitly Parallel Instruction Set Computing (EPIC) IA-64 multimedia instructions are semantically compatible with MMX and Streaming SIMD Extensions instructions
L1 cache	32KB L1 cache (16KB instruction cache and 16KB data cache) / integrated in die / full speed / 4-way set associative / 32 byte cache line / unpublished data path / parity protected / 2 cycle latency
L2 cache	96KB L2 cache (unified) / integrated in die / full speed / 6-way set associative 64 byte cache line / 256-bit data path (32 bytes) / L2 tag parity protected / L2 data is ECC protected / 6 cycle latency (with the 2 cycle L1 miss) / 9 cycle latency for floating point loads
L3 cache	2MB or 4MB L3 cache (unified) / off die, on cartridge / full speed / 4-way set associative / 64 byte cache line / 128-bit data path (16 bytes) / L2 tag and data is ECC protected / 21 cycle latency / 24 cycle latency for floating point loads
Front Side Bus Memory addressability	266MHz (double pumped 133MHz bus) / 64-bit data path / ECC / cache line size is chipset dependent 44-bit address bus for 18TB memory addressability / 256MB maximum page size / Merced limited to 36-bit addressability or 64GB (460GX also limits to 64GB) / compatible with flat 64-bit address model with 18EX (18 exabytes) memory addressability, but chipset dependent
Execution units Floating point Registers Out-of-order instructions	2 integer units, 2 memory units, 2 floating point units, 3 branch exection units / able to execute 4 ALU instructions per clock / 2 loads or stores per clock / 9 issue ports Each floating point unit contains a Floating Point Multiply Accumulate (FMAC) that operates on 82-bit operands / each FMAC unit can execute two floating point operations per clock with single, double and double-extended precision 128 integer registers, 128 floating point registers, 8 branch registers, 64 1-bit predicate registers No / 10 stage in-order pipeline
EPIC features	Predication: speculatively executes instructions along both branch paths and then discards the results not needed Speculation: speculatively loads data before needed and still tries to find the data in the caches first Compiler: reorders and optimizes instruction stream at compile time Bundle: uses three 41-bit instructions and an 5-bit template into a 128-bit fixed length bundle Register stacking: reduces call/return procedure overhead via the flexible integer register model managed by the Register Stack Engine (RSE) Register rotation: automatically renames registers in hardware to improve software loop performance
Compatibility Multiple processors Systems management	Native IA-64 support / IA-32 instruction compatibility in hardware Initial version supports up to 4-way SMP support Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron) Transistors Package type Connector Frequency (MHz) and available date	0.18u ~25 million in die (core) / ~300 million in die and L3 cache 418-pin array cartridge (418PAC) Requires 418-pin Low Insertion Force (LIF) Socket M and one Power Pod per processor 733MHz with 2MB L3 cache (available July 2001) 733MHz with 4MB L3 cache (available July 2001) 800MHz with 2MB L3 cache (available July 2001) 800MHz with 4MB L3 cache (available July 2001)
Chipset support	Intel 460GX with SDRAM PC100 memory (limits to 36-bit addressing to 64GB memory addressability))

McKinley A-64 (Intel Architecture 64-bit) / Explicitly Parallel Instruction Set Computing (EPIC) / Intel Itanium architecture A-64 multimedia instructions are semantically compatible with MMX and Streaming SIMD Extensions instructions 32KB L1 cache (16KB instruction cache and 16KB data cache) / integrated in die / full speed / 4-way set associative / write-through data cache / 64 byte cache line / unpublished data path / parity protected / 1 cycle latency 256KB L2 cache (unified) / integrated in die / full speed / 8-way set associative / write-back / 128 byte cache line / 256-bit data path (32 bytes) / L2 data and L2 tag is ECC protected / 5 cycle latency / 6 cycle latency for floating point loads
write-through data cache / 64 byte cache line / unpublished data path / parity protected / 1 cycle latency 256KB L2 cache (unified) / integrated in die / full speed / 8-way set associative / write-back / 128 byte cache line / 256-bit data path (32 bytes) / L2 data and L2 tag is ECC protected /
128 byte cache line / 256-bit data path (32 bytes) / L2 data and L2 tag is ECC protected /
1.5MB or 3MB L3 cache (unified) / integrated in die / full speed / 12-way set associative / write-back / 128 byte cache line / 128-bit data path (16 bytes) / L3 tag and data is ECC protected / 12 cycle latency
400MHz (quad pumped 100MHz bus) / 128-bit data path / 6.4GB/sec throughput / ECC / cache line size is chipset dependent
compatible with flat 64-bit address model with 18EX (18 exabytes) memory addressability, but chipset dependent
4 memory/ALU/multimedia units, 2 integer/ALU/multimedia units, 2 load units, 2 store units, 3 branch units, 2 extended-precision floating point units, 1 single-precision floating point unit / able to execute 6 instructions per clock / 2 loads and stores per clock / 11 issues ports 128 integer registers, 128 floating point registers, 8 branch registers, 64 1-bit predicate registers No / 8 stage in-order pipeline
Predication: speculatively executes instructions along both branch paths and then discards the results not needed Speculation: speculatively loads data before needed and still tries to find the data in the caches first Compiler: reorders and optimizes instruction stream at compile time Bundle: uses three 41-bit instructions and an 5-bit template into a 128-bit fixed length bundle Register stacking: reduces call/return procedure overhead via the flexible integer register model managed by the Register Stack Engine (RSE) Register rotation: automatically renames registers in hardware to improve software loop performance
Native IA-64 support / IA-32 instruction compatibility in hardware Natively supports up to 8-way SMP support / enabled for >8-way SMP Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
0.18u 611-pin array cartridge (PAC611) Requires mPGA700 Zero Insertion Force (ZIF) Socket and one Power Pod per processor 900MHz with 1.5MB L3 cache (available July 2002) 1GHz with 1.5MB L3 cache (available July 2002) 1GHz with 3MB L3 cache (available July 2002)
Intel E8870 chipset, OEM custom chipset, IBM XA-64™ chipset
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¹ Intel 64 Technology (formerly EM64T):

Intel 64 Technology (formerly Intel EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel 64 Technology. Processor will not operate (including 32-bit operation) without an Intel 64 Technology-enabled BIOS. Performance will vary depending on your hardware and software configurations.

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