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Personal Systems Reference Intel PC Processors - withdrawn

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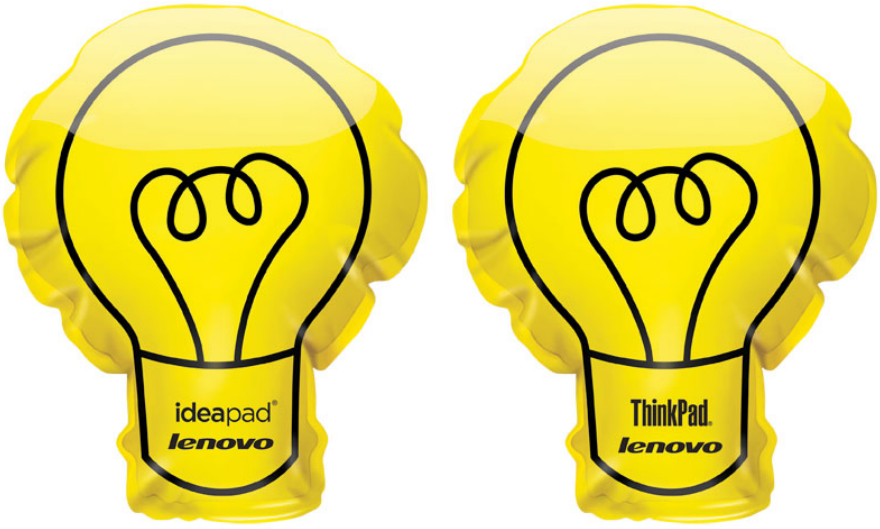

lenovo.com

PC Processors (486 family)

	80486SX	*80486SX2*	*80486SL*	*80486DX*	*80486DX2*
Vendor	Intel®	Intel	Intel	Intel	Intel
Code name	**P23**		**H4C**	**P4**	**P24**
Type	CISC	CISC	CISC	CISC	CISC
Avail date	Available now	Available April 94	Available now	Available now	Available now
MHz	16, 20, 25, 33MHz	50/25MHz	25, 33MHz	25, 33, 50MHz	66/33, 50/25, 40/20MHz
iCOMP	100 at 25MHz	180 at 50/25MHz	166 at 33MHz	249 at 50MHz	297 at 66/33MHz
Data bus	32-bit Data Path	32-bit Data Path	32-bit Data Path	32-bit Data Path	32-bit Data Path
Processor	32-bit Processor	32-bit Processor	32-bit Processor	32-bit Processor	32-bit Processor
Address bus	32-bit Address Path	32-bit Address Path	32-bit Address Path	32-bit Address Path	32-bit Address Path
Cache	8KB unified cache Write-thru 4 way set	8KB unified cache Write-thru 4 way set	8KB unified cache Write-thru 4 way set	8KB unified cache Write-thru 4 way set	8KB unified cache Write-thru 4 way set
Features			Math cop optional (ThinkPad 350 have none: ThinkPad 750 has one)	Math coprocessor std	Math coprocessor std
	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) * 168 pin / 1.0u	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 0.8u	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 1.0u	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 1.0u	Optimized instructions Address pipelining Burst mode bus Power mgmt (SMM) 168 pin / 0.8u
Voltage	5.0 or 3.3 volts	5.0 volts	**3.3 volts**	5.0 volts	5.0 volts
OverDrive upgrade	① 486SX2 ② 486DX2 ③ IntelDX4 ④ P24T (Pentium)	① 486DX2 ② IntelDX4 ③ P24T (Pentium)	None	① 486SX2 ② 486DX2 ③ IntelDX4 ④ P24T (Pentium)	① IntelDX4 ② P24T (Pentium)

	IntelDX4 ™	*IntelDX4*
Vendor	Intel	Intel
Code name	**P24C**	**P24D**
Type	CISC	CISC
Avail date	Available April 94	4th quarter 1995
MHz	100/50, 100/33, 83/33, 75/25	
iCOMP	435 at 100MHz	
Data bus	32-bit Data Path	32-bit Data Path
Processor	32-bit Processor	32-bit Processor
Address bus	32-bit Address Path	32-bit Address Path
Cache	**16KB** unified cache Write-thru 2 way set; with parity	**16KB** unified cache **Write-back** 4 way set
Features	Math coprocessor std	Math coprocessor std
	Optimized instructions Address pipelining Burst mode bus (to 160MB/sec) Power mgmt (SMM) 168 pin / 0.6u	Optimized instructions Address pipelining Burst mode bus (to 160MB/sec) Power mgmt (SMM) 168 pin / 0.6u
Voltage	**3.3 volts**	**3.3 volts**
OverDrive upgrade	235/237 pin P24CT based on Pentium technology; 100/50 and 100/33MHz; Available 1996	235/237 pin P24CT based on Pentium technology; 100/50 and 100/33MHz; Available 1996

* Effective June 1993, the **486SX**, **486DX**, and **486DX2** (called 'SL Enhanced Intel486™ microprocessors') includes the **486SL** power mgmt technology called System Management Mode (SMM).

Intel OverDrive™ Processor: with a single chip upgrade, gives up to a 70% performance boost w/o modifying external system clock or memory subsystem. The chip may be placed in an open socket on planar or in the socket after the existing processor is removed.

Burst mode bus: for reads and writes from processor to memory; 4 back-to-back data transfers (usually in 5 cycles); 486 is 128-bits (16 bytes) and Pentium CPU is 256-bits (64-bits x 4; (32 bytes).

(2INTEL) Compiled by Roger Dodson, IBM. October 1998

Mobile Intel® Celeron® Processor		
Vendor	Intel®	*Same*
Positioning	Value mobile PC	*Same*
Instruction architecture	IA-32 / P6 microarchitecture / CISC/RISC/micro-ops	*Same*
MMX™ / Streaming SIMD	Yes / 57 new instructions / eight 64-bit MMX registers	MMX (57 new instructions) / **Streaming SIMD Extensions** (70 new instructions)
L1 cache - size	**16KB data; 16KB instruction**	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)	*Same*
L1 cache - bus	64-bit / full speed / non-blocking	*Same*
L1 cache - parity	Parity in cache and internal registers	*Same*
L2 cache - size	**128KB** (integrated on the die)	*Same*
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect	*Same*
L2 cache - organization	4 way set associative / non-blocking	*Same*
L2 cache - bus	**Full speed** / 64-bit path / ECC	*Same*
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - speed	**66MHz Frontside Bus**	**100MHz Frontside Bus**
System bus - features	Nonblocking cache hierarchy	*Same*
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture	*Same*
Execution units	2 integer/MMX units; 1 floating pt unit;1 load unit; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history) / 512 entry BTB	*Same*
Speculative execution	Yes	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width) / 32-bit word size	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (64GB physical address space; 64TB virtual)	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks)	*Same*
Power management	System Management Mode (SMM)	*Same*
Multiple processors	No SMP support	*Same*
Technology (micron)	**0.25u**	**0.18u**
CPU voltage	1.6 volts (2.5 volts I/O); 1.5 volts (2.5 volts I/O) for 266MHz low voltage;	1.6 volts (2.5 volts I/O); 1.35 volts (2.5 volts I/O) for Low Voltage processors; 1.1 volts for 500MHz Ultra Low Voltage processors
Power	Supports QuickStart allowing 0.4 watt idle power state	Supports QuickStart allowing 0.4 watt idle power state
Transistors	~18 million	~18 million
Package type	280-pin Mobile Module (MMC1) 400-pin Mobile Module (MMC2) 240-pin Mini-cartridge Ball Grid Array (BGA) Micro Pin Grid Array (Micro-PGA)	280-pin Mobile Module (MMC1) 400-pin Mobile Module (MMC2) 240-pin Mini-cartridge Ball Grid Array (BGA) Micro Ball Grid Array (Micro-BGA2) Micro Pin Grid Array (Micro-PGA or Micro-PGA2)
Frequency (available)	**266/66MHz (low voltage)** (April 1999) **266/66MHz** (January 1999) **300/66MHz** (January 1999) **333/66MHz** (April 1999) **366/66MHz** (May 1999) **400/66MHz** (June 1999) **433/66MHz** (Sept 1999) **466/66MHz** (Sept 1999)	**400A/100MHz Low Voltage** (February 2000) **450/100MHz** (February 2000) **500/100MHz** (February 2000) **500/100MHz Ultra Low Voltage** (January 2001) **550/100MHz** (April 2000) **500/100MHz Low Voltage** (June 2000) **600/100MHz** (June 2000) **600/100MHz Ultra Low Voltage** 1.1v (May 2001) **600/100MHz Low Voltage** 1.35v (May 2001) **650/100MHz** (June 2000) **700/100MHz** (September 2000) **750/100MHz** (March 2001) **800/100MHz** (May 2001) **850/100MHz** (July 2001) **900/100MHz** (October 2001)
Chipset support	**440DX, 440BX, 440MX, 440ZX, 440ZX-66**	**440DX, 440BX, 440MX, 440ZX, 440ZX-66, 815EM**

Celeron® is based on the same P6 core architecture as the Pentium II

PC Processors (Mobile Celeron) - Fall 2001

Mobile Intel® Celeron® Processor		
Vendor	Intel®	*Same*
Positioning	Value mobile PC	*Same*
Instruction architecture	IA-32 / P6 microarchitecture / CISC/RISC/micro-ops	*Same*
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - size	**16KB data; 16KB instruction**	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4-way set associative	*Same*
L1 cache - bus	64-bit / full speed / non-blocking	*Same*
L1 cache - parity	Parity in cache and internal registers	*Same*
L2 cache - size	**128KB / full speed**	**256KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	64-bit data path / ECC	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering		Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) / Data Prefetch Logic
L2 cache - organization	8-way set associative / non-blocking	8-way set associative
L2 cache - controller	Integrated / unified (internal die; on die)	Integrated / unified (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type		Non-blocking / pipelined burst synchronous
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - speed	**133MHz frontside bus**	**100MHz or 133MHz frontside bus**
System bus - features	Nonblocking cache hierarchy	*Same*
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture	*Same*
Execution units	2 integer/MMX units; 1 floating pt unit;1 load unit; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history) / 512 entry BTB	*Same*
Speculative execution	Yes	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width) / 32-bit word size	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (64GB physical address space; 64TB virtual)	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks)	*Same*
Power management	Quick Start and Deep Sleep	*Same*
Multiple processors	No SMP support	*Same*
Technology (micron)	**0.18u**	**0.13u**
CPU voltage	1.7 volts	1.1 volts for Ultra Low Voltage processors 1.15 volts for Low Voltage processors 1.4 or 1.45 volts for others
Package type	Micro-Flip Chip Ball Grid Array (Micro-FCBGA) Micro-Flip Chip Pin Grid Array (Micro-FCPGA)	Micro-Flip Chip Ball Grid Array (Micro-FCBGA) Micro-Flip Chip Pin Grid Array (Micro-FCPGA)
Frequency (available)	**733MHz** (October 2001) **800A MHz** (October 2001) **866MHz** (October 2001) **933MHz** (October 2001) *The "A" is added to the "800A" in Micro-FCBGA and Micro-FCPGA to distinguish it from the Mobile Intel Celeron Processor 800MHz in Micro-BGA2 and Micro-PGA2 packages*	**650/100MHz Ultra Low Voltage** (January 2002) **650/100MHz Low Voltage** (October 2001) **700MHz/100MHz Ultra Low Voltage** (September 2002) **733MHz/133MHz Low Voltage** (April 2002) **733MHz/133MHz Ultra Low Voltage** (September 2002) **800MHz/133MHz Ultra Low Voltage** (January 2003) **866MHz/133MHz Low Voltage** (January 2003) **1GHz/133MHz** (April 2002) **1.06GHz/133MHz** (January 2002) **1.13GHz/133MHz** (January 2002) **1.2GHz/133MHz** (January 2002) **1.33GHz/133MHz** (June 2002)

Mobile Intel Celeron Processor (Northwood)

Mobile Intel® Celeron® for value mobile systems

Code name	**Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	AutoHALT, Stop-Grant, Sleep, Deep Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Voltage	1.3 volts
Package and connector	**Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket**
Frequency (MHz) and available date	1.26GHz available April 2003 1.4GHz available June 2002 1.5GHz available June 2002 1.6GHz available September 2002 1.7GHz available September 2002 1.8GHz available September 2002 2.0GHz available January 2003 2.2GHz available April 2003 2.4GHz available June 2003 2.5GHz available November 2003
Chipset support	**Intel 845MZ with DDR-SDRAM memory** **Intel 845MP with DDR-SDRAM memory** **Intel 852GM, 852GME, 852PM with DDR-SDRAM memory** **Other compatible chipsets**

(27INTEL) Compiled by Roger Dodson, IBM. November 2003

[Mobile] Intel Celeron M Processor

Intel® Celeron® M processor for mobile systems

Code name	Banias Celeron or ICP-M
Messaging	Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**

		Voltage	*Thermal Design Power*	*Announce date*
Frequency (MHz/GHz) and available date	**800MHz Ultra Low Voltage**	**1.004 volts**	**7 watts**	January 2004
	900MHz Ultra Low Voltage	**1.004 volts**	**7 watts**	April 2004
	1.2GHz	**1.356 volts**	**24.5 watts**	January 2004
	1.3GHz	**1.356 volts**	**24.5 watts**	January 2004
	1.4GHz	**1.356 volts**	**24.5 watts**	April 2004

Chipset support	**Intel 855 chipset family** **Intel 852GM** **Other compatible chipsets**

[Mobile] Intel Celeron M Processor 3xx

Intel® Celeron® M processor for mobile systems

	Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Available date
Intel Celeron M Processor Ultra Low Voltage 353	900MHz	512KB	No	400MHz	No	July 2004
Intel Celeron M Processor Ultra Low Voltage 373	1.0GHz	512KB	**Yes**	400MHz	No	January 2005
Intel Celeron M Processor Ultra Low Voltage 383	1.0GHz	**1MB**	**Yes**	400MHz	No	April 2005
Intel Celeron M Processor 310	1.2GHz	512KB	No	400MHz	No	January 2004
Intel Celeron M Processor 320	1.3GHz	512KB	No	400MHz	No	January 2004
Intel Celeron M Processor 330	1.4GHz	512KB	No	400MHz	No	April 2004
Intel Celeron M Processor 340	1.5GHz	512KB	No	400MHz	No	June 2004
Intel Celeron M Processor 350	1.3GHz	**1MB**	No	400MHz	No	August 2004
Intel Celeron M Processor 350J	1.3GHz	**1MB**	**Yes**	400MHz	No	August 2004
Intel Celeron M Processor 360	1.4GHz	**1MB**	No	400MHz	No	August 2004
Intel Celeron M Processor 360J	1.4GHz	**1MB**	**Yes**	400MHz	No	August 2004
Intel Celeron M Processor 370	1.5GHz	**1MB**	**Yes**	400MHz	No	January 2005
Intel Celeron M Processor 380	1.6GHz	**1MB**	**Yes**	400MHz	No	July 2005
Intel Celeron M Processor 390	1.7GHz	**1MB**	**Yes**	400MHz	No	January 2005

Code name	Banias Celeron or ICP-M
Messaging	Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	No
Hyper-Threading	No
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
Execute Disable Bit	*Some:* protects memory data from malicious software execution
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**512KB** or **1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	*310 to 340:* 130nm (nanometer) or 0.13u (micron); *350 to 360:* 90nm or 0.09u
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**

Frequency			*Voltage*	*Thermal Design Power*
	353:	**900MHz Ultra Low Voltage**	**0.0940 volts**	**5 watts**
	373/383:	**1.0GHz Ultra Low Voltage**	**0.0940 volts**	**5 watts**
	310:	**1.2GHz**	**1.356 volts**	**24.5 watts**
	320:	**1.3GHz**	**1.356 volts**	**24.5 watts**
	330:	**1.4GHz**	**1.356 volts**	**24.5 watts**
	340:	**1.5GHz**	**1.356 volts**	**24.5 watts**
	350/350J:	**1.3GHz**	**1.260 volts**	**21 watts**
	360/360J:	**1.4GHz**	**1.260 volts**	**21 watts**
	370:	**1.5GHz**	**1.260 volts**	**21 watts**
	380:	**1.6GHz**	**1.260 volts**	**21 watts**
	390:	**1.7GHz**	**1.260 volts**	**27 watts**

Chipset support
Intel 852GM chipset
Intel 855 chipset family
Mobile Intel 910GML Express Chipset
Mobile Intel 915 and 945 Express Chipset family
Other compatible chipsets

Intel® Celeron® M processor for mobile systems	**Clock Speed**	**L2 cache**	**System bus MHz**	**Core**	**Hyper-Threading Technology**	**Total threads (logical)**	**Virtual-ization Tech**	**Execute Disable Bit**	**Enhanced Intel SpeedStep™ Technology**	**Intel 64 Tech**	**Avail-able date**
Intel Celeron M Processor Ultra Low Voltage 423	1.06GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Apr 2006
Intel Celeron M Processor Ultra Low Voltage 443	1.20GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Jan 2007
Intel Celeron M Processor 410	1.46GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	May 2006
Intel Celeron M Processor 420	1.60GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Apr 2006
Intel Celeron M Processor 430	1.73GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Apr 2006
Intel Celeron M Processor 440	1.86GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Sep 2006
Intel Celeron M Processor 450	2.00GHz	1MB	533MHz	Single	No	1	No	Yes	No	No	Sep 2006

Processor generation	**Yonah**
Marketing name	**Intel Celeron M Processor**
Core	Single-core
Centrino™	Not part of the Centrino branding
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep low power C-states
Thermal management	Thermal management system (digital temperature sensor and thermal monitor)
Hyper-Threading	None
Total threads	One thread (one cores with no Hyper-Threading support provides one logical processor)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	None
Virtualization Technology	None
L1 cache - bus	256-bit data path, full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**1MB** / full speed / Advanced Transfer Cache / Data Cache Unit Streamer
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	**533MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 266MHz
System bus - width	64-bit data path
Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Power	*Ultra Low Voltage:* 5.5 watts; *420/430:* 27 watts
Package and connector	Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball) [Ultra Low Voltage offered only in Micro Flip-Chip Ball Grid Array (Micro-FCBGA)]
Chipset support	**Mobile Intel 945 Express Chipset family**, Mobile Intel 940GML Express Chipset, other compatible chipsets

PC Processors (Celeron)

Celeron®		
Code name	**Covington**	**Mendocino**
Vendor	Intel®	*Same*
Positioning	Value PC desktops	*Same*
Instruction architecture	IA-32 / P6 microarchitecture / CISC/RISC/micro-ops	*Same*
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers	*Same*
Streaming SIMD	None	566MHz and higher: Streaming SIMD Extensions
L1 cache - controller	Integrated	*Same*
L1 cache - size	**16KB data; 16KB instruction**	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4-way set associative (data); 2-way set associative (instructn)	*Same*
L1 cache - bus	64-bit / full speed	*Same*
L1 cache - type; parity	Non-blocking; parity in cache and internal registers	*Same*
L2 cache - controller	None	Integrated
L2 cache - size	None	**128KB** (integrated on the die)
L2 cache - write policy	N/A	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - organization	N/A	4 way set associative / non-blocking
L2 cache - bus	None	**Full speed** / ECC
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - speed	**66MHz**	**66MHz or 100MHz**
System bus - features	Nonblocking cache hierarchy	*Same*
	8 entry transactional buffer for system bus	*Same*
Bus architecture	Frontside bus only since no L2 cache (backside bus) / no Dual Independent Bus Architecture (DIB)	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture
Execution units	2 integer/MMX units; 1 floating point unit; 1 load; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history)	*Same*
Speculative execution	Yes	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width); 32-bit word size	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (64GB physical address space; 64TB virtual)	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks) / Addr-data-data-data-data	*Same*
Multiple processors	**No SMP support**	*Same*
Technology	0.25u CMOS	0.25u (Flip-Chip is 0.18u)
Die area	139.9 sq mm	153.9 sq mm
CPU voltage	2.0 volt core	*Same*
Transistors	~7.5 million	~19 million (core is ~7.5 million)
Package type	**Single Edge Processor (SEP) package requires Intel Slot 1**	**- SEP for Slot 1** (266, 300, 300A, 333, 366, 400, 433MHz) **- Plastic Pin Grid Array (PPGA) for 370 pin socket** (300A, 333, 366, 400, 433, 466, 500, 533MHz) **- Flip-Chip Pin Grid Array (FC-PGA) for 370 pin** (533A, 566, 600, 633, 667, 700, 733, 766, 800, 850, 900, 950MHz, 1GHz, 1.10 GHz)
Available date	May 1998	August 1998 (300A and 366); Jan 1999 (366 and 400) March 1999 (433); April 1999 (466); August 99 (500); January 2000 (533); March 2000 (566 and 600); June 2000 (633, 677, 700); November 2000 (733, 766); January 2001 (800); April 2001 (850); July 2001 (900); August 2001 (950, 1GHz, 1.10GHz)
Frequency	**266MHz, 300MHz / 66MHz system bus**	**300AMHz, 333MHz, 366MHz, 400MHz, 433MHz, 466MHz, 500MHz, 533MHz, 533A, 566MHz, 600MHz, 633MHz, 667MHz, 700MHz, 733MHz, 766MHz / all have 66MHz Frontside bus** **766 , 800, 850, 900, 950MHz, 1GHz, 1.10 GHz / 100MHz Frontside bus**
Chipset support	**440EX is preferred (does support 440LX, 440BX)**	**440ZX-66, 810, 810E, 810E2, 815, 815E, 815EP is preferred (does support 440EX, 440LX, or 440BX)**

Celeron® is based on the same P6 core architecture as the Pentium II

The "A" is added to the "300A" to distinguish it as having L2 cache as the "300"MHz version does not have L2 cache

The "A" is added to the "533A" to distinguish it as having FC-PGA packaging as the "533"MHz version uses SEP packaging

(9INTEL) Compiled by Roger Dodson, IBM. September 2001

PC Processors (Celeron - Tualatin)

Celeron®	
Code name	**Tualatin**
Vendor	Intel®
Positioning	Value PC desktops
Instruction architecture	IA-32 / P6 microarchitecture / CISC/RISC/micro-ops
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers
Streaming SIMD	Streaming SIMD Extensions
L1 cache - controller	Integrated
L1 cache - size	**16KB data; 16KB instruction**
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4-way set associative (data); 2-way set associative (instruction)
L1 cache - bus	64-bit / full speed
L1 cache - type; parity	Non-blocking; parity in cache and internal registers
L2 cache - size	**256KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	8-way set associative
L2 cache - controller	Integrated / unified (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type	Non-blocking / pipelined burst synchronous
System bus - parity	ECC on system bus; parity on address bus (frontside)
System bus - speed	**100MHz Frontside Bus**
System bus - features	Nonblocking cache hierarchy 8 entry transactional buffer for system bus
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus architecture
Execution units	2 integer/MMX units; 1 floating point unit; 1 load; 1 store unit
Pipeline stages	Decoupled, 14 stage superpipelined
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes
Math coprocessor	Pipelined math coprocessor
Internal processing	32-bits (300 bit internal bus width); 32-bit word size
External data bus	64-bit system bus with ECC
External address bus	36-bits (64GB physical address space; 64TB virtual)
User registers	8 GPR, 8 FP, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks) / Addr-data-data-data-data
Multiple processors	**No SMP support**
Technology	0.13u process technology
Package type	**Flip-Chip Pin Grid Array 2 (FC-PGA2)** for 370-pin zero insertion force socket (PGA370 socket)
Available date	October 2001 (1.20GHz) January 2002 (1.30GHz) June 2002 (1.40GHz)
Frequency	**1.20 GHz / 100MHz Frontside bus** **1.30 GHz / 100MHz Frontside bus** **1.40 GHz / 100MHz Frontside bus**
Chipset support	**Intel 440BX, 440ZX, 810 series, 815, series, and others**

Intel® Celeron® for value desktop systems

Code name	**Willamette**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) / Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**128KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Frontside bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.18u
Transistors	~42 million with die size of 217 square millimeters
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	1.7GHz available May 2002 1.8GHz available June 2002
Chipset support	**Intel 845 family**

[Desktop] Intel Celeron Processor (Northwood)

Intel® Celeron® for value desktop (and mobile) systems

Code name	**Celeron Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) / Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**128KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Frontside bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	2.0GHz available September 2002 2.1GHz available November 2002 2.2GHz available November 2002 2.2GHz available June 2003 for mobile systems 2.3GHz available March 2003 2.3GHz available June 2003 for mobile systems 2.4GHz available March 2003 2.4GHz available June 2003 for mobile systems 2.5GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.6GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.7GHz available September 2003 for both desktop and mobile systems (transportable processors) 2.8GHz available November 2003 for both desktop and mobile systems (transportable processors)
Chipset support	**Intel 845 and 865 desktop family and others** **Intel 852GM, 852GME, 852PM mobile chipset**

(28INTEL) Compiled by Roger Dodson, IBM. November 2003

[Desktop] Intel Celeron D Processor 3xx

Intel® Celeron® D Processor for desktop systems

	Clock speed	L2 cache	System bus	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Process	Available date
Intel Celeron D Processor 320	2.40GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processor 325	2.53GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processor 325J	2.53GHz	256KB	533MHz	**Yes**	No	No	No	90nm	June 2004
Intel Celeron D Processor 326	2.53GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	May 2005
Intel Celeron D Processor 330	2.66GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processor 330J	2.66GHz	256KB	533MHz	**Yes**	No	No	No	90nm	June 2004
Intel Celeron D Processor 331	2.66GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	May 2005
Intel Celeron D Processor 335	2.80GHz	256KB	533MHz	No	No	No	No	90nm	June 2004
Intel Celeron D Processor 335J	2.80GHz	256KB	533MHz	**Yes**	No	No	No	90nm	June 2004
Intel Celeron D Processor 336	2.80GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	May 2005
Intel Celeron D Processor 340	2.93GHz	256KB	533MHz	No	No	No	No	90nm	September 2004
Intel Celeron D Processor 340J	2.93GHz	256KB	533MHz	**Yes**	No	No	No	90nm	September 2004
Intel Celeron D Processor 341	2.93GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	May 2005
Intel Celeron D Processor 345	3.06GHz	256KB	533MHz	No	No	No	No	90nm	November 2004
Intel Celeron D Processor 345J	3.06GHz	256KB	533MHz	**Yes**	No	No	No	90nm	November 2004
Intel Celeron D Processor 346	3.06GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	May 2005
Intel Celeron D Processor 347	3.06GHz	**512KB**	533MHz	**Yes**	No	No	**Yes**	**65nm**	October 2006
Intel Celeron D Processor 350	3.20GHz	256KB	533MHz	**Yes**	No	No	No	90nm	June 2005
Intel Celeron D Processor 351	3.20GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	June 2005
Intel Celeron D Processor 352	3.20GHz	**512KB**	533MHz	**Yes**	No	No	**Yes**	**65nm**	May 2006
Intel Celeron D Processor 355	3.33GHz	256KB	533MHz	**Yes**	No	No	**Yes**	90nm	December 2005
Intel Celeron D Processor 356	3.33GHz	**512KB**	533MHz	**Yes**	No	No	**Yes**	**65nm**	May 2006
Intel Celeron D Processor 360	3.46GHz	**512KB**	533MHz	**Yes**	No	No	**Yes**	**65nm**	Sept 2006
Intel Celeron D Processor 365	3.60GHz	**512KB**	533MHz	**Yes**	No	No	**Yes**	**65nm**	January 2007

Processor generation	**Prescott** (90nm) or **Cedar Mill** (65nm)
Core	Single-core; based on Prescott (Pentium 4) core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	No
Execute Disable Bit	*Some:* protects memory data areas from malicious software execution
Intel 64 Technology[1]	*Some:* Intel 64 Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** or **512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**533MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Process technology	*Prescott:* 90nm (nanometer) or 0.09u (micron); *Cedar Mill:* 65nm (nanometer) or 0.065u (micron)
Package and socket	*All:* **Flip-Chip Pin Grid Array (FC-mPGA4) package requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket** *All except 320 and 350:* **775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T)
Chipset support	*FC-mPGA4 package:* Intel 845 family, 848P, 865 family, 910, or other compatible chipsets *FC-LGA4 package:* Intel 910 and 915 Express Chipset family

PC Processors (Pentium)

	Pentium®	Pentium	Pentium	Pentium	Pentium
Code name	**P5**	**P54C**	**P54LM (120, 133, and 150 MHz is P54CSLM)**	**P54CQS**	**P54CS**
Vendor	Intel®	*Same*	*Same;*	*Same*	*Same*
Positioning	Strong performance; Software compatibility	*Same*	**Mobile systems**	*Same*	*Same*
Instruction architecture	CISC/RISC	*Same*	*Same*	*Same*	*Same*
Cache	8KB data; 8KB instruction	*Same*	*Same*	*Same*	*Same*
Cache - write policy	Write-back or thru (data) Write-thru (instruction)	*Same*	*Same*	*Same*	*Same*
Cache - organization	2 way set associative (both)	*Same*	*Same*	*Same*	*Same*
Cache - parity	Parity in cache	*Same*	*Same*	*Same*	*Same*
Parity	Parity on all external data and address transfers	*Same*	*Same*	*Same*	*Same*
Execution units	2 fixed point units and 1 floating point unit	*Same*	*Same (in block)* **Lower voltage (2.9 v) Pentium used for mobile computing (with no OverDrive). Uses Voltage Reduction Technology (VRT)**	*Same (in block)* **QS means Quick Shrink. Shrink of chip using .35u process, but left on P54C packaging size**	*Same (in block)* **Same .35 as P54CQS but now also reduced packaging size from P54C/ P54CQS of 253 mm to 142 mm**
Superscalar issue	2 integers per cycle or 2 floating point per cycle	*Same*			
Superscalar execution	2 integers per cycle or 2 floating point per cycle	*Same*			
Out-of-order instruct	No	*Same*			
Branch prediction	Dynamic (based on history)	*Same*			
Speculative execution	No	*Same*			
Math coprocessor	Pipelined math coprocessor	*Same*			
Internal processing	32-bits	*Same*	*Same*	*Same*	*Same*
External data bus	64-bits	*Same*	*Same*	*Same*	*Same*
External address bus	32-bits	*Same*	*Same*	*Same*	*Same*
Word size	32-bits	*Same*	*Same*	*Same*	*Same*
User registers	8 GPR, 8 FP stack	*Same*	*Same*	*Same*	*Same*
Cache line size	32 bytes	*Same*	*Same*	*Same*	*Same*
Burst mode bus	Addr-data-data-data-data	*Same*	*Same*	*Same*	*Same*
Power management	System Management Mode (SMM)	*Same*	*Same*	*Same*	*Same*
Multiple processors	Requires external chip set design	Multiple processor ready via built in APIC	*Same*	*Same*	*Same*
Die area	294 sq mm	146 sq mm (original); 228 sq mm (Level C2)	*Same*	135 sq mm (active) w/ 253 sq mm die	142 sq mm
Technology	0.8u BiCMOS	0.6u BiCMOS	*Same*	0.35u BiCMOS	*Same*
Supply voltage	5.0 volts	3.3 volts	2.9 volts internal but 3.3 v external	3.3 volts	*Same*
Power (typical/max)	13/16 watts	4/10 watts	4/8 watts	4/10 watts (120/60)	5.4/14.5 (166/66)
Transistors	3.1 million	*Same*	*Same*	*Same*	*Same*
Package	273 pin grid array	296 pin grid array or TCP for 90/60 and 75/50MHz	Tape Carrier Package (TCP)	296 pin grid array	*Same*
Available date	June 1993	March 1994	May 1995	March 1995	October 1995
Frequency	60, 66MHz	75/50, 90/60, 100/66, and 120/60MHz	75/50, 90/60, 100/66, 120/60, 133/66 and 150/60MHz	120/60, 133/66MHz	133/66, 150/60, 166/66, and 200/66MHz
OverDrive® upgrade	P5T uniprocessor; 273 pin; available 1996	P54CT uniprocessor; 320 pin; available 1996 and Pentium OverDrive with MMX technology for 75/50, 90/60, and 100/66 available March 1997	None	P54CT for 120/60; P54CTB for 133/66MHz	P54CTB (none for 200MHz)

(5INTEL) Compiled by Roger Dodson, IBM. October 1998

PC Processors (Pentium - MMX)

	Pentium® Processor with MMX™ Technology	Pentium Processor with MMX Technology	
Code name	**P55C**	**P55CLM**	**P55CSLM / Tillamook**
Vendor	Intel®	*Same*	*Same*
Positioning	**Desktop systems**	**Notebook systems**	*Same*
Instruction architecture	CISC/RISC	*Same*	*Same*
MMX technology	Yes / 57 new instructions	*Same*	*Same*
L1 cache	16KB data; 16KB instruction	*Same*	*Same*
L1 cache - write policy	Write-back or thru (data) Write-thru (instruction)	*Same*	*Same*
L1 cache - organization	4 way set associative (both)	*Same*	*Same*
L1 cache - parity	Parity in cache	*Same*	*Same*
Parity	Parity on all external data and address transfers	*Same*	*Same*
Execution units	2 fixed point units and 1 floating point unit	*Same*	*Same*
Superscalar issue	2 integers per cycle or 2 floating point per cycle	*Same*	*Same*
Superscalar execution	2 integers per cycle or 2 floating point per cycle	*Same*	*Same*
Out-of-order instruct	No	*Same*	*Same*
Branch prediction	Dynamic (based on history); improved over P54C and P54CS	*Same*	*Same*
Speculative execution	No	*Same*	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*	*Same*
Internal processing	32-bits	*Same*	*Same*
External data bus	64-bits	*Same*	*Same*
External address bus	32-bits	*Same*	*Same*
Word size	32-bits	*Same*	*Same*
User registers	8 GPR, 8 FP stack	*Same*	*Same*
Cache line size	32 bytes	*Same*	*Same*
Burst mode bus	Addr-data-data-data-data	*Same*	*Same*
Power management	System Management Mode (SMM)	*Same*	*Same*
Multiple processors	Multiple processor ready via built in APIC	*Same*	*Same*
Die area	141 sq mm	*Same*	95 sq mm
Technology	0.35u CMOS	*Same*	0.25u CMOS
Supply voltage	2.8 volts internal / 3.3 v external	2.45 volts internal / 3.3 volts ext	1.8 volts internal / 2.5 volts ext 266: 2.0 volts internal / 2.5 v ext
Power	16 watts max at 200 MHz; 17 watts for 233MHz	8 watts max at 166MHz	3.9 watts max at 233MHz
Transistors	4.5 million	*Same*	*Same*
Package	273 pin grid array (PGA) Pin compatible with non-MMX Pentiums except different core voltage	Tape Carrier Package (TCP) or Mobile Module	Tape Carrier Package (TCP) or 280-pin Mobile Module (MMC1)
Available date	January 1997 for 166, 200; June 1997 for 233MHz	January 1997 for 150, 166MHz; May 1997 for 133MHz	Sept 1997 for 200, 233MHz; January 1998 for 166, 266MHz; January 1999 for 300MHz
Frequency	**166/66, 200/66, 233/66MHz**	**133/66, 150/60, 166/66MHz**	**166/66, 200/66, 233/66, 266/66, and 300/66MHz**
OverDrive® upgrade	None	None	None

PC Processors (Pentium Pro)

Pentium® Pro	
Code name	**P60** (.6 micron); **P6S** (.35 micron)
Vendor	Intel®
Positioning	Strong performance; Software compatibility
Instruction architecture	CISC/RISC/micro-ops
L1 cache - size	8KB data; 8KB instruction
L1 cache - write policy	Write-back or thru (data) Write-thru (instruction)
L1 cache - organization	4 way set associative (data) 2 way set associative (instruction)
L1 cache - parity	Parity in cache and internal registers
L2 cache - size	256KB or 512KB or 1MB (external die)
L2 cache - write policy	Write-through or write-back (programmable per line)
L2 cache - organization	4 way set associative
L2 cache - bus	On dedicated full speed bus / 64-bit path
L2 cache - parity	Error Checking and Correcting (ECC)
Parity - external bus	ECC on data bus; parity on address bus (frontside)
Features	Nonblocking cache hierarchy Independent backside and frontside buses operate concurrently
Memory bus	8 entry transactional buffer for memory bus
Execution units	2 integer units; 1 floating point unit; 1 load unit; 1 store unit
Pipeline stages	Decoupled, 14 stage superpipelined
Superscalar dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Internal processing	32-bits
External data bus	64-bits
External address bus	36-bits (address 64GB)
Word size	32-bits
User registers	8 GPR, 8 FP, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks)
Burst mode bus	Addr-data-data-data-data
Power management	System Management Mode (SMM)
Multiple processors	Multiple processor ready via built in APIC
Die area	306 (150) or 197 sq mm (CPU); 202 or 242 sq mm (L2)
Technology	0.6u (150), 0.35u (others); four layer metal BiCMOS
Supply voltage	2.9 volts
Power (typical/maximum)	23/29 watts (150MHz)
Transistors	5.5 million in core + 15.5 (256) or 31 (512) million in L2
Package	387 pin dual cavity PGA
Available date	late 1995; mid 1996 for 200MHz with 512KB August 1997 for 200MHz with 1MB
Frequency	**150/60, 180/60, 200/66MHz with 256KB L2 cache;** **166/66, 200/66MHz with 512KB L2 cache;** **200/66 MHz with 1MB L2 cache**
Performance	327 SPECint92; 7.29 SPECint95 at 180MHz; 220 SPECfp92; 6.08 SPECint95 at 180MHz
OverDrive® upgrade	150, 180MHz support Pentium II OverDrive at 300MHz 166, 200MHz support Pentium II OverDrive at 333MHz

Nonblocking cache hierarchy - 486 and Pentium are blocking; meaning an L2 cache miss causes processor to stall. P6 does not stall on an L2 cache miss, but can do other useful work

Frontside bus - external 64-bit memory bus

Backside bus - 64-bit bus to integrated L2 cache

Transaction buffer - while the Pentium Pro is waiting for a memory access to complete, it can begin another access. As many as 8 of these transactions can be outstanding

Micro-ops - decoders break down CISC instructions into simpler operations that resemble RISC instructions. Micro-ops are easier to dispatch and execute in parallel than their complex x86 counterparts

x86 instructions (8 to 120 bits long) go through three parallel decoders to translate into single micro-ops (complex ones into 1 to 4 micro-ops). Micro-ops are 118 bits long

(6INTEL) Compiled by Roger Dodson, IBM. October 1998

PC Processors (Mobile Pentium II)

Mobile Pentium® II		
Code name	**Deschutes**	**Dixon**
Vendor	Intel®	*Same*
Positioning	Mobile systems	*Same*
Instruction architecture	CISC/RISC/micro-ops	*Same*
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers	*Same*
L1 cache - controller	Integrated	*Same*
L1 cache - size	**16KB data; 16KB instruction**	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)	*Same*
L1 cache - bus	64-bit / full speed / non-blocking	*Same*
L1 cache - parity	Parity in cache and internal registers	*Same*
L2 cache - controller	Integrated	*Same*
L2 cache - size	**512KB** / unified (external die)	**256KB** / unified **(on die)**
L2 cache - write policy	Write-through or write-back (programmable per line)	*Same*
L2 cache - organization	4 way set associative / non-blocking	*Same*
L2 cache - bus	**Half speed bus** (or 1/3 speed) / 64-bit path	**Full speed bus** (or 1/3 speed) / 64-bit path
L2 cache - type	Non-blocking / pipelined burst synchronous	*Same*
L2 cache - parity	ECC	*Same*
System bus - speed	**66MHz**	*Same*
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - features	Nonblocking cache hierarchy 8 entry transactional buffer for system bus	*Same* *Same*
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)	*Same*
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches	*Same*
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width)	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (64GB physical address space; 64TB virtual)	*Same*
Word size	32-bits	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks)	*Same*
Burst mode bus	Addr-data-data-data-data	*Same*
Power management	System Management Mode (SMM)	*Same*
Multiple processors	Not supported	*Same*
Technology	**0.25u; five layer metal CMOS**	**0.25u; 400MHz is 0.18u and 0.25u**
CPU voltage	1.6 volts (3.3 volt I/O)	1.6 volts (2.5 volt I/O); 1.5v for 266MHz low voltage and 400MHz
Power (total in watts)	8.6 watts (supports QuickStart allowing 0.4 watt idle power state)	366MHz: 9.5 watts; 6.6 watts typical (5.8 watts for 266MHz low voltage); supports QuickStart allowing 0.4 watt idle power state
Transistors	~7.5 million	~27 million (366MHz)
Package type	**280-pin Mobile Module (MMC1)** **400-pin Mobile Module (MMC2)** **240-pin Mini-cartridge**	**280-pin Mobile Module (MMC1)** **400-pin Mobile Module (MMC2)** **240-pin Mini-cartridge** **Ball Grid Array (BGA)** **Micro PGA**
Available date	April 1998 (233 and 266MHz); September 1998 (300MHz)	January 1999; April 1999 (266MHz low voltage); June 1999 (400MHz)
Frequency (clock/system)	**233/66MHz with half speed L2 cache bus** **266/66MHz with half speed L2 cache bus** **300/66MHz with half speed L2 cache bus**	**266/66MHz low voltage with full speed L2 bus** **266PE/66MHz with full speed L2 cache bus** **300PE/66MHz with full speed L2 cache bus** **333/66MHz with full speed L2 cache bus** **366/66MHz with full speed L2 cache bus** **400/66MHz with full speed L2 cache bus**
Chipset support	**440BX**	**440BX, 440MX**

The "PE" is added to the 266PE and 300PE to distinguish these speeds from the half speed 512KB L2 cache versions.

Nonblocking cache hierarchy - 486 and Pentium are blocking; meaning an L2 cache miss causes processor to stall. Pentium II does not stall on an L2 cache miss, but can do other useful work

Frontside bus - external 64-bit memory (system) bus

Backside bus - 64-bit bus to integrated L2 cache

Transaction buffer - while the Pentium II is waiting for a memory access to complete, it can begin another access. As many as 8 of these transactions can be outstanding

Micro-ops - decoders break down CISC instructions into simpler operations that resemble RISC instructions. Micro-ops are easier to dispatch and execute in parallel than their complex x86 counterparts

x86 instructions (8 to 120-bits long) go through three parallel decoders to translate into single micro-ops (complex ones into 1 to 4 micro-ops). Micro-ops are 118 bits long

PC Processors (Pentium II)

Pentium® II		
Code name	**Klamath**	**Deschutes**
Vendor	Intel®	*Same*
Positioning	Desktop systems; entry servers	*Same*
Instruction architecture	CISC/RISC/micro-ops	*Same*
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers	*Same*
L1 cache - controller	Integrated	*Same*
L1 cache - size	16KB data; 16KB instruction	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)	*Same*
L1 cache - bus	64-bit / full speed	*Same*
L1 cache - type	Non-blocking	*Same*
L1 cache - parity	Parity in cache and internal registers	*Same*
L2 cache - controller	Integrated	*Same*
L2 cache - size	512KB / unified (external die)	*Same*
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect	*Same*
L2 cache - organization	4 way set associative / non-blocking	*Same*
L2 cache - bus	Dedicated 1/2 or 1/3 speed bus / 64 bit path	*Same*
L2 cache - type	Non-blocking / pipelined burst synchronous	*Same*
L2 cache - parity	Non-ECC or ECC on 233 and 266MHz / ECC on all 300MHz	**ECC**
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - speed	66MHz	**66 or 100MHz**
System bus - features	Nonblocking cache hierarchy	*Same*
	8 entry transactional buffer for system bus	*Same*
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)	*Same*
Execution units	2 integer/MMX units; 1 floating point unit;1 load unit; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches	*Same*
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width)	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (4 GB physical address space; 64 TB virtual)	*Same*
Word size	32-bits	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks)	*Same*
Burst mode bus	Addr-data-data-data-data	*Same*
Power management	System Management Mode (SMM)	*Same*
Multiple processors	Glueless 2 way SMP via built in APIC	*Same*
Die area	**203 sq mm (CPU) / 560 mils/side**	**131 sq mm (CPU) / ~429 x 474 mils/side**
Technology	**0.35u; four layer metal CMOS**	**0.25u; five layer metal CMOS**
CPU voltage	2.0 or 2.8 volts	**2.0 volts**
Power (plate/total in watts)	33.6/34.8 (233MHz), 37.0/38.2 (266), 41.4/43.0 (300)	19.4/23.6 (333 MHz), 20.2/24.5 (350), 26.7/27.9 (400)
Transistors	~7.5 million	*Same*
Package type	**Single Edge Contact Cartridge (SECC) requires Intel Slot 1**	**SECC or SECC2 requires Intel Slot 1**
Package size (of SEC)	5.505 inches x 2.473 inches x 0.647 inches	*Same*
	528 pin plastic land-grid array (LGA) package	*Same*
Available date	Apriil 1997 (233 and 266MHz); August 1997 (300MHz)	January 1998 (333MHz); April 1998 (350, 400MHz) August 1998 (450MHz)
Frequency (clock/system)	**233/66MHz with 117MHz L2 cache bus**	**333/66MHz with 166MHz L2 cache bus**
	266/66MHz with 133MHz L2 cache bus	**350/100MHz with 175MHz L2 cache bus**
	300/66MHz with 150MHz L2 cache bus	**400/100MHz with 200MHz L2 cache bus**
		450/100MHz with 225MHz L2 cache bus
Chipset support	**440FX, 440LX**	**440FX, 440LX, 440BX, 440GX**
OverDrive® upgrade	No OverDrive expected	No OverDrive expected

(7INTEL) Compiled by Roger Dodson, IBM. October 1998

PC Processors (Pentium II Xeon)

Pentium® II Xeon™	
Code name	**Deschutes Slot 2 or DS2P**
Vendor	Intel®
Positioning	Mid-range and higher servers and workstations
Instruction architecture	CISC/RISC/micro-ops
MMX technology	Yes / 57 new instructions / eight 64-bit MMX registers
L1 cache - controller	Integrated
L1 cache - size	16KB data; 16KB instruction
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L1 cache - bus	64-bit / full speed
L1 cache - type	Non-blocking
L1 cache - parity	Parity in cache and internal registers
L2 cache - controller	Integrated
L2 cache - size	**512KB, 1MB,** or **2MB** / unified (external die) / CSRAM
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - organization	4 way set associative / non-blocking
L2 cache - bus	Dedicated full speed bus / 64-bit path
L2 cache - type	Non-blocking / pipelined burst synchronous
L2 cache - parity	ECC
System bus - parity	ECC on system bus; parity on address bus (frontside)
System bus - speed	**100MHz**
System bus - features	Nonblocking cache hierarchy 8 entry transactional buffer for system bus
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Pipeline stages	Decoupled, 14 stage superpipelined
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Internal processing	32-bits (300-bit internal bus width)
External data bus	64-bit system bus with ECC
External address bus	36-bits (64GB physical address space (PSE-36); 64TB virtual)
Word size	32-bits
User registers	8 GPR, 8 FP, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks)
Burst mode bus	Addr-data-data-data-data
Power management	System Management Mode (SMM)
Systems management	SMBus for thermal sensor, PIROM, Scratch EEPROM
Multiple processors	**1-, 2-, 4-, and 8-way SMP support**
Die area	**131 sq mm (CPU), 560 mils/side / 222 sq mm (L2 cache)**
Technology	**0.25u; five layer metal CMOS**
CPU voltage	1.8 to 2.8 volts
Transistors	~7.5 million
Package type	**Single Edge Contact (SEC) cartridge requires Intel Slot 2 (SC330)**
Package size (of SEC)	4.992 inches high x 6.000 inches wide x 0.733 inches
Available date	July 1998 (400MHz), October 1998 (450MHz)
Frequency	**400/100MHz with 400MHz L2 cache bus and 512KB L2 cache** **400/100MHz with 400MHz L2 cache bus and 1MB L2 cache** **450/100MHz with 450MHz L2 cache bus and 512KB L2 cache** **450/100MHz with 450MHz L2 cache bus and 1MB L2 cache** **450/100MHz with 450MHz L2 cache bus and 2MB L2 cache**
Chipset support	**450NX (servers) or 440GX (workstations)**

(3INTEL) Compiled by Roger Dodson, IBM. January 1999

PC Processors (Pentium III)

Intel® Pentium® III for desktop and entry servers					
MHz	**450, 500, 550, 600**	**533B, 600B**	**500E, 550E**	**600E, 650, 700, 750, 800, 850, 1.0GHz**	**533EB, 600EB, 667, 733, 800EB, 866, 933, 1.0BGHz, 1.13GHz**
Code name	**Katmai**		**Coppermine (or Coppermine-T)**		
Instruction architecture	CISC/RISC/micro-ops				
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)				
L1 cache - bus	64-bit / full speed				
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking				
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)				
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)				
L2 cache - size	**512KB / half speed**		**256KB / full speed** (Advanced Transfer Cache)		
L2 cache - data path	**64-bit data path / ECC**		**256-bit data path / quad-wide cache line / ECC**		
L2 cache - buffering	**None**		**Intelligent buffering of read and stores** (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries)		
L2 cache - organization	4-way set associative		8-way set associative		
L2 cache - controller	Integrated / unified (external die)		Integrated / unified (internal die; on die)		
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect				
L2 cache - type	Non-blocking / pipelined burst synchronous				
System bus - speed	**100MHz**	**133MHz**	**100MHz**	**100MHz**	**133MHz**
Memory addressability	4GB memory addressability		64GB memory addressability		
System bus - width	64-bit system bus with ECC				
System bus - parity	ECC on system bus; parity on address bus (frontside bus)				
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit				
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined				
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)				
Superscalar retire	3 micro-ops per cycle				
Out-of-order instructions	Yes (called dynamic execution)				
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches				
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)				
Math coprocessor	Pipelined math coprocessor				
Serial number	**Unique processor serial number**				
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)				
Internal processing	32-bits (300 bit internal bus width)				
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming				
Cache line size	32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data				
Power management	System Management Mode (SMM)				
Multiple processors	Glueless 2-way SMP via built in APIC		None	Glueless 2-way SMP via built in APIC	
Technology (micron)	0.25u	0.25u	0.18u	0.18u	0.18u
Transistors	~9.5 million for processor core	~28.1 million	~28.1 million	~28.1 million	~28.2 million
Package type Connector	**Single Edge Contact Cartridge (SECC) or Single Edge Contact Cartridge 2 (SECC2)**		**FC-PGA (Flip-Chip Pin Grid Array)**	**Single Edge Contact Cartrdg 2 (SECC2) or Flip-Chip Pin Grid Array (FC-PGA)** (800, 800EB, 1 and 1.13GHz only SECC2)	
Available date	**Requires Intel Slot 1** March 1999 (450 and 500MHz), May 1999 (550MHz), August 1999 (600MHz)	**Requires Intel Slot 1** September 1999	**Socket 370** October 1999	**Requires Intel Slot 1 or Socket 370** October 1999, Dec 1999 (750, 800) Mar 2000 (850), Jun 2001 (1.0, 1.1)	October 1999, Dec 1999 (800EB), Mar 2000 (866), Mar 2000 (1.0GHz) May 2000 (933) July 2000 (1.13GHz)
Frequency (MHz)	450 with 100MHz FSB 500 with 100MHz FSB 550 with 100MHz FSB 600 with 100MHz FSB	533B with 133 FSB 600B with 133 FSB	500E with 100 FSB 550E with 100 FSB	600E w/ 100 FSB 650 with 100 FSB 700 with 100 FSB 750 with 100 FSB 800 with 100 FSB 1.0 with 100 FSB 1.1 with 100 FSB	533EB with 133 FSB 600EB with 133 FSB 667 with 133 FSB 733 with 133 FSB 800EB with 133 FSB 933 with 133 FSB 1.0BGHz with133FSB 1.13GHz with133FSB
Chipset support	**440BX, 440GX, 810, 810E, 820, 840**	**810E, 820, 840**	**440BX, 440GX, 810x, 815x, 820x, 840**	**440BX, 440GX, 810x, 815x, 820x, 840**	**810x, 815x, 820x, 840**

B = 133MHz Frontside Bus (system bus) to main memory
E = 256KB full speed L2 cache (Advanced Transfer Cache with Advanced System Buffering)
L2 cache bus also called Backside Bus
Memory or system bus also called Frontside Bus

(10INTEL) Compiled by Roger Dodson, IBM. June 2001

PC Processors (Pentium III - Tualatin)

Intel® Pentium® III for desktop and entry-level workstations and servers

Code name	**Tualatin** (pronounced "TWO-ala-tin")
Instruction architecture	IA-32 / CISC/RISC/micro-ops
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - bus	64-bit / full speed
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L2 cache - size	**256** or **512KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	8-way set associative
L2 cache - controller	Integrated / unified (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type	Non-blocking / pipelined burst synchronous
Frontside bus - speed	**133MHz**
Memory addressability	64GB memory addressability
System bus - width	64-bit system bus with ECC
System bus - parity	ECC on system bus; parity on address bus (frontside bus)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Processor serial number	None
Serial number	Unique processor serial number
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Internal processing	32-bits (300 bit internal bus width)
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data
Power management	System Management Mode (SMM)
Multiple processors	**Some support 2-way SMP with appropriate chipset support**
Technology (micron)	**0.13u**
Package type	**Flip-Chip Pin Grid Array-2 (FC-PGA2)**
Connector	**Requires Socket 370 (PGA370)**
Frequency (MHz)	**900 MHz Ultra Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers** (announced Jan 2003) **933 MHz Low Voltage with 512KB L2 cache for blade servers** (announced September 2002) **1.0A GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announced August 2001) **1.0 GHz Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers** (announced January 2003) **1.13A GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announced August 2001) **1.13 GHz-S 512KB L2 cache for servers** (announced June 2001) **1.20 GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announce August 2001) **1.26 GHz-S 512KB L2 cache for servers** (announced August 2001) **1.4 GHz-S 512KB L2 cache for servers and blade servers** (announced January 2002)
Chipset support	**Intel 815x, 820x, 840 and others** **ServerWorks® HE-SL and others**
Server blade support	Pentium III at 933MHz and 1.4GHz supported in "Performance Server Blades"

L2 cache bus also called Backside Bus
Memory or system bus also called Frontside Bus

Intel® Mobile Pentium® III	
Code name	**Coppermine**
Positioning	Mobile systems
Instruction architecture	CISC/RISC/micro-ops
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - bus	64-bit / full speed
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L2 cache - size	**256KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	**Intelligent buffering of read and stores** (called Advanced System Buffering with 4 write-back buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	8-way set associative
L2 cache - controller	Integrated controller / unified L2 cache (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type	Non-blocking / pipelined burst synchronous
System bus - speed	**100MHz Frontside Bus**
System bus - width	64-bit system bus with ECC
System address bus	36-bits (4GB memory cacheability; 64GB memory addressability)
System bus - parity	ECC on system bus; parity on address bus (frontside bus)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Pipeline stages	Decoupled, 14 stage superpipelined
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter; ave of 5 branches)
Math coprocessor	Pipelined math coprocessor
Serial number	**Unique processor serial number**
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Internal processing	32-bits (300 bit internal bus width) / 32-bit word size
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks)
Burst mode bus	Addr-data-data-data-data
Multiple processors	None
Technology (micron)	**0.18u**
CPU voltage	1.1-1.7 volts (2.5 volt I/O); 1.6v typical (except 1.35v for some low-power versions); 500MHz Ultra Low Voltage is 1.1v typical (0.975v battery optimized)
Power management	QuickStart and Deep Sleep modes for low-power dissipation
Transistors	~28.1 million
Package type	**400-pin Mobile Module (MMC2), 240-pin Mini-cartridge, Ball Grid Array (BGA2), or Micro PGA2**
Available date	Oct 1999 for 400, 450, 500MHz; Jan 2000 for 500MHz (1.35v), 600, 650MHz; April 2000 for 700MHz; June 2000 for 600 (1.35v), 750MHz; Sept 200 for 800 and 850MHz; Jan 2001 for 500MHz (1.1v); Feb 2001 for 700MHz (1.1v), Mar 2001 for 900MHz and 1GHz; May 2001 for 600MHz (1.1v) and 750MHz (1.35v)
Frequency (MHz)	**400MHz** **450MHz** **500MHz** **500MHz Low Voltage (1.35v)** **500MHz Ultra Low Voltage (1.1v) (with Intel SpeedStep™ tech);** 300MHz in Battery Optimized Mode (0.975v) **600MHz Ultra Low Voltage (1.1v) (with Intel SpeedStep tech);** 300MHz in Battery Optimized Mode (0.975v) **600MHz (with Intel SpeedStep™ technology);** 500MHz in Battery Optimized Mode **600MHz Low Voltage (1.35v) (with Intel SpeedStep tech);** 500MHz in Battery Optimized Mode **650MHz (with Intel SpeedStep technology);** 500MHz in Battery Optimized Mode **700MHz Low Voltage (1.35v) (with Intel SpeedStep technology);** 500MHz in Battery Optimized Mode (1.1v) **700MHz (with Intel SpeedStep technology);** 550MHz in Battery Optimized Mode **750MHz Low Voltage (1.35v) (with Intel SpeedStep technology);** 500MHz in Battery Optimized Mode (1.1v) **750MHz (with Intel SpeedStep technology);** 600MHz in Battery Optimized Mode **800MHz (with Intel SpeedStep technology);** 650MHz in Battery Optimized Mode **850MHz (with Intel SpeedStep technology);** 700MHz in Battery Optimized Mode **900MHz (with Intel SpeedStep technology);** 700MHz in Battery Optimized Mode **1GHz (with Intel SpeedStep technology);** 700MHz in Battery Optimized Mode
Chipset support	**440BX, 440MX, 440ZX-M, 815EM**

Non-blocking cache hierarchy - 486 and Pentium are blocking; meaning an L2 cache miss causes processor to stall. Pentium II and III do not stall on an L2 cache miss, but can do other useful work

Frontside bus - external 64-bit memory (system) bus

Backside bus - 256-bit bus to integrated L2 cache

Transaction buffer - while the Pentium II and Pentium III are waiting for a memory access to complete, it can begin another access. As many as 8 of these transactions can be outstanding

SpeedStep - processor operates at full speed in Maximum Performance Mode (on AC power) and reduced speed in Battery Optimized Mode (on battery)

PC Processors (Mobile Intel Pentium III-M)

Mobile Intel® Pentium® III Processor-M for mobile systems (and server blade systems)

Code name	**Tualatin** (pronounced "TWO-ala-tin")
Instruction architecture	IA-32 / CISC/RISC/micro-ops
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
Technology	Enhanced Intel SpeedStep™ technology
L1 cache - bus	64-bit / full speed
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L2 cache - size	**512KB / full speed** (Advanced Transfer Cache) / integrated / unified (internal die; on die)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) / Data Prefetch Logic
L2 cache - organization	8-way set associative / non-blocking / pipelined burst synchronous
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
Frontside bus - speed	**133MHz** (some at 100MHz)
Memory addressability	64GB memory addressability
System bus - width	64-bit system bus with ECC
System bus - parity	ECC on system bus; parity on address bus (frontside bus)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined
Superscalar issue/retire	Issues 6 micro-ops per cycle (3 micro-ops is typical) / retires 3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Serial number	Unique processor serial number
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Internal processing	32-bits (300 bit internal bus width)
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data
Power management	Quick Start, Deep Sleep, Deeper Sleep
Multiple processors	No SMP support (2-way SMP for 800MHz Low Voltage for server blade systems with ServerWorks® ServerSet III LE)
Technology (micron)	0.13u (130-nanometer)
Package type	Micro-FCPGA (Flip-Chip Pin Grid Array) for socketable boards Micro-FCBGA (Flip-Chip Ball Grid Array) for surface mount boards

L2 cache bus also called Backside Bus
Memory or system bus also called Frontside Bus

		Frontside bus	*Maximum Performance Mode*	*Battery Optimized Mode*	*Announce date*
Frequency (MHz)	**700MHz Ultra Low Voltage***	**100MHz**	**700MHz at 1.1V**	**300MHz at 0.95V**	October 2001/Nov 2001*
	733MHz Low Voltage	**133MHz**	**733MHz at 1.15V**	**466MHz at 1.05V**	October 2001
	750MHz Ultra Low Voltage	**100MHz**	**750MHz at 1.1V**	**350MHz at 0.95V**	January 2002
	750MHz Low Voltage	**100MHz**	**750MHz at 1.15V**	**450MHz at 1.05V**	October 2001
	800A MHz Low Voltage	**100MHz**	**800MHz at 1.15V**	**500MHz at 1.05V**	October 2001
	800MHz Low Voltage**	**133MHz**	**800MHz at 1.15V**	**533MHz at 1.05V**	October 2001/Mar 2002**
	800MHz Ultra Low Voltage*	**100MHz**	**800MHz at 1.15V**	**400MHz at 1.05V**	April 2002*
	800MHz Ultra Low Voltage*	**133MHz**	**800MHz at 1.15V**	**400MHz at 1.05V**	April 2002*
	850MHz Low Voltage	**133MHz**	**850MHz at 1.15V**	**500MHz at 1.05V**	January 2002
	850MHz Ultra Low Voltage	**100MHz**	**850MHz at 1.1V**	**400MHz at 0.95V**	September 2002
	866MHz Low Voltage	**133MHz**	**866MHz at 1.15V**	**533MHz at 1.05V**	January 2002
	866MHz	**133MHz**	**866MHz at 1.40V**	**667MHz at 1.15V**	July 2001
	866MHz Ultra Low Voltage	**133MHz**	**866MHz at 1.1V**	**400MHz at 0.95V**	September 2002
	900MHz Ultra Low Voltage	**100MHz**	**900MHz at 1.1V**	**400MHz at 0.95V**	January 2003
	933MHz Ultra Low Voltage	**133MHz**	**933MHz at 1.1V**	**400MHz at 0.95V**	January 2003
	933MHz Low Voltage	**133MHz**	**933MHz at 1.15V**	**533MHz at 1.05V**	April 2002
	933MHz	**133MHz**	**933MHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1GHz	**133MHz**	**1GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1GHz Low Voltage	**133MHz**	**1GHz at 1.15V**	**533MHz at 1.05V**	September 2002
	1.06GHz	**133MHz**	**1.06GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1.13GHz	**133MHz**	**1.13GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1.2GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	October 2001
	1.26GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	September 2002
	1.33GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	September 2002

Chipset support	**Intel 830MP, 830M, 830MG and others**
Server blade support	*** Supported in server blade systems; Micro-FCBGA only; uses Intel 440GX chipset**
	**** Announced March 2002 for server blade systems; Micro-FCBGA only; supports 2-way SMP in server blade systems with ServerWorks ServerSet III LE chipset**

Mobile Intel Pentium 4-M Processor

Mobile Intel® Pentium® 4 Processor-M for mobile systems

Code name	**Mobile Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	*Some:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Stop Grant, Sleep, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400** or **533MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	*400MHz:* **Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket** *533MHz:* **Micro Flip-Chip Pin Grid Array (uFCPGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket**

		System bus	*Maximum Performance Mode*	*Battery Optimized Mode*	*Hyper-Threading (HT) Technology*	*Announce date*
Frequency (MHz)	**1.4GHz**	**400MHz**	1.4GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.5GHz	**400MHz**	1.5GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.6GHz	**400MHz**	1.6GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		March 2002
	1.7GHz	**400MHz**	1.7GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		March 2002
	1.8GHz	**400MHz**	1.8GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.9GHz	**400MHz**	1.9GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2002
	2.0GHz	**400MHz**	2.0GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2002
	2.2GHz	**400MHz**	2.2GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		Sept 2002
	2.4GHz	**400MHz**	2.4GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		Jan 2003
	2.5GHz	**400MHz**	2.5GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2003
	2.6GHz	**400MHz**	2.6GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2003
	2.40GHz	**533MHz**	2.40GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.66GHz	**533MHz**	2.66GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.80GHz	**533MHz**	2.80GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	3.06GHz	**533MHz**	3.06GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.66GHz	**533MHz**	2.66GHz at 1.525v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	2.80GHz	**533MHz**	2.80GHz at 1.525v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	3.06GHz	**533MHz**	3.06GHz at 1.55v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	3.2GHz	**533MHz**	3.2GHz at 1.55 volts	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003

Chipset support	**Intel 845MZ with DDR-SDRAM memory** **Intel 845MP with DDR-SDRAM memory** **Intel 852GM, 852GME, 852PM with DDR-SDRAM memory**

[Mobile] Intel Pentium M Processor

Intel® Pentium® M processor for mobile systems

Code name	**Banias**
Branding	Part of the Intel Centrino™ mobile technology when included with an Intel 855 family chipset and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**

Frequency (MHz/GHz) and available date		*Highest Frequency Mode*	*Lowest Frequency Mode*	*Announce date*
	900MHz Ultra Low Voltage	**900MHz at 1.0 volts**	**600MHz at 0.85 volts**	March 2003
	1.0GHz Ultra Low Voltage	**1.0GHz at 1.0 volts**	**600MHz at 0.85 volts**	June 2003
	1.1GHz Ultra Low Voltage	**1.1GHz at 1.0 volts**	**600MHz at 0.85 volts**	April 2004 (also Pentium M 713)
	1.1GHz Low Voltage	**1.1GHz at 1.18 volts**	**600MHz at 0.96 volts**	March 2003
	1.2GHz Low Voltage	**1.2GHz at 1.18 volts**	**600MHz at 0.96 volts**	June 2003
	1.3GHz Low Voltage	**1.3GHz at 1.18 volts**	**600MHz at 0.96 volts**	April 2004 (also Pentium M 718)
	1.3GHz	**1.3GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.4GHz	**1.4GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.5GHz	**1.5GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.6GHz	**1.6GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.7GHz	**1.7GHz at 1.5 volts**	**600MHz at 0.96 volts**	June 2003

Chipset support	**Intel 855 chipset family with DDR-SDRAM memory** **Other compatible chipsets**

[Mobile] Intel Pentium M Processor 7xx

Intel® Pentium® M processor for mobile systems

	Clock speed Performance Mode	Clock speed Battery Mode	L2 cache	Execute Disable Bit	System bus	Technology	Available date
Intel Pentium M Processor Ultra Low Voltage 713	1.10GHz	600MHz	**1MB**	No	400MHz	130nm	April 2004
Intel Pentium M Processor Ultra Low Voltage 723	1.00GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Ultra Low Voltage 733	1.10GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Ultra Low Voltage 733J	1.10GHz	600MHz	2MB	**Yes**	400MHz	90nm	August 2004
Intel Pentium M Processor Ultra Low Voltage 753	1.20GHz	600MHz	2MB	**Yes**	400MHz	90nm	January 2005
Intel Pentium M Processor Ultra Low Voltage 773	1.30GHz	600MHz	2MB	**Yes**	400MHz	90nm	January 2006
Intel Pentium M Processor Low Voltage 718	1.30GHz	600MHz	**1MB**	No	400MHz	130nm	April 2004
Intel Pentium M Processor Low Voltage 738	1.40GHz	600MHz	2MB	No	400MHz	90nm	July 2004
Intel Pentium M Processor Low Voltage 758	1.50GHz	600MHz	2MB	**Yes**	400MHz	90nm	January 2005
Intel Pentium M Processor Low Voltage 778	1.60GHz	600MHz	2MB	**Yes**	400MHz	90nm	July 2005
Intel Pentium M Processor 705	1.50GHz	600MHz	**1MB**	No	400MHz	130nm	July 2004
Intel Pentium M Processor 705a*	1.50GHz	600MHz	**1MB**	No	400MHz	130nm	November 2004
Intel Pentium M Processor 710	1.40GHz	600MHz	2MB	No	400MHz	90nm	October 2004
Intel Pentium M Processor 715	1.50GHz	600MHz	2MB	No	400MHz	90nm	June 2004
Intel Pentium M Processor 715a*	1.50GHz	600MHz	2MB	No	400MHz	90nm	January 2005
Intel Pentium M Processor 725	1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2004
Intel Pentium M Processor 725a*	1.60GHz	600MHz	2MB	No	400MHz	90nm	June 2005
Intel Pentium M Processor 730	1.60GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	January 2005
Intel Pentium M Processor 735	1.70GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 740	1.73GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	January 2005
Intel Pentium M Processor 745	1.80GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 750	1.86GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	January 2005
Intel Pentium M Processor 755	2.00GHz	600MHz	2MB	No	400MHz	90nm	May 2004
Intel Pentium M Processor 760	2.00GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	January 2005
Intel Pentium M Processor 765	2.10GHz	600MHz	2MB	No	400MHz	90nm	October 2004
Intel Pentium M Processor 770	2.13GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	January 2005
Intel Pentium M Processor 780	2.26GHz	**800MHz**	2MB	**Yes**	**533MHz**	90nm	July 2005

*requires improved processor cooling because of higher Thermal Design Power

Code name	**Dothan** (705, 705a, 713, and 718 are Banias)
Branding	Part of the **Intel Centrino™ mobile technology** when included with an Intel 855 or 915 Express Chipset family and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	**Enhanced Intel SpeedStep™ technology**, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
Hyper-Threading	No
Execute Disable Bit	*Some:* protects memory data areas from malicious software execution
Intel 64 Technology[1]	None
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**1MB** or **2MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400** or **533MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Technology (micron)	0.09 micron or 90 nanometer (*705, 705a, 713, and 718:* 0.13 micron or 130 nanometer)
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**
Chipset support	**Intel 855 , 910, and 915 Express Chipset family** **Other compatible chipsets**

PC Processors (Pentium III Xeon)

Intel® Pentium® III Xeon™		
Code name	**Tanner**	**Cascades**
Positioning	Mid-range and higher servers and workstations	Same
Instruction architecture	CISC/RISC/micro-ops	Same
MMX™ / Streaming SIMD	MMX / Streaming SIMD Extensions (SIMD)	Same
L1 cache - bus	64-bit / full speed	Same
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking	Same
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	Same
L1 cache - organization	4-way set associative (data); 2-way set associative (instruction)	Same
L1 cache - parity	Parity in cache and internal registers	Same
L2 cache - size / speed	**512KB, 1MB, or 2MB / full speed**	**256KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	64-bit path / ECC	**256-bit data path / quad-wide cache line** / ECC
L2 cache - buffering	None	**Intelligent buffering of read and stores** (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	4 way set associative	8-way set associative
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect	Same
L2 cache - controller	Integrated / unified L2 cache (external die) / CSRAM	Integrated controller / unified (internal die; on die)
L2 cache - type	Non-blocking / pipelined burst synchronous	Same
System bus - speed	**100MHz**	**133MHz**
System bus - width	64-bit system bus with ECC	Same
System address bus	36-bits (4GB memory cacheability; 64GB memory addressability) / PSE-36 / Intel Extended Server Memory Architecture (PSE-36)	Same
System bus - parity	ECC on system bus; parity on address bus (frontside bus)	Same
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit	Same
Pipeline stages	Decoupled, 14 stage superpipelined	Same
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	Same
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	Same
Superscalar retire	3 micro-ops per cycle	Same
Out-of-order instructions	Yes (called dynamic execution)	Same
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches	Same
Speculative execution	Yes (typically 20 to 30 instructions beyond counter; 5 average)	Same
Math coprocessor	Pipelined math coprocessor	Same
Voltage regulation	External Voltage Regulation Module (VRM)	**On-Cartridge Voltage Regulation**
Serial number	Unique processor serial number (software-accessible)	Same
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)	Same
Internal processing	32-bits (300 bit internal bus width)	Same
Word size	32-bits	Same
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming	Same
Cache line size	32 bytes (8 bytes x 4 chunks)	Same
Burst mode bus	Addr-data-data-data-data	Same
Systems management	SMBus for thermal sensor, PIROM, Scratch EEPROM	Same
Multiple processors	**1-, 2-, 4-, and 8-way SMP support**	**1- and 2-way SMP support**
Technology (micron)	0.25u or 0.18u	**0.18u**
Transistors	~7.5 million	~28.1 million
Package type	**Single Edge Contact Cartridge (SECC) requires Intel Slot 2 (SC330)** 4.992 inches high x 6.000 inches wide x 0.733 inches	Same
Available date	April 1999 (500 and 550MHz/512KB), September 1999 (550MHz/1 and 2MB), May 2000 (700MHz/1 and 2MB), March 2001 (900MHz/2MB)	October 1999 (600, 667, 733MHz), January 2000 (800MHz), March 2000 (866MHz) August 2000 (1GHz)
Frequency (MHz)	**500/100MHz with 512KB L2 cache** **500/100MHz with 1MB L2 cache** **500/100MHz with 2MB L2 cache** **550/100MHz with 512KB L2 cache** **550/100MHz with 1MB L2 cache** **550/100MHz with 2MB L2 cache** **700/100MHz with 1MB L2 cache** **700/100MHz with 2MB L2 cache** **900/100MHz with 2MB L2 cache** (uses same Advanced Transfer Cache of Cascades of 256-bit L2 data path with Advanced System Buffering)	**600/133MHz with 256KB L2 cache** **667/133MHz with 256KB L2 cache** **733/133MHz with 256KB L2 cache** **800/133MHz with 256KB L2 cache** **866/133MHz with 256KB L2 cache** **1GHz/133MHz with 256KB L2 cache** **450NX (servers), 440GX (workstations), 840**
Chipset support	**450NX (servers), 440GX (workstations), or Profusion™**	

Intel® Pentium® 4 for high performance desktop systems

	1.3GHz, 1.4GHz, 1.5GHz, 1.6GHz, 1.7GHz, 1.8GHz, 1.9GHz, 2.0GHz
Code name	**Willamette**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Front Side Bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Front Side Bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.18u
Transistors	~42 million with die size of 217 square millimeters
Package and connector	1. **Pin Grid Array (PGA) requires 423-pin Zero Insertion Force (ZIF) socket named Intel Socket 423 (PGA423); used with RDRAM-based 850 chipset** 2. **Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	1.3GHz: 423-pin available January 2001 1.4GHz: 423-pin available November 2000 1.5GHz: 423-pin available November 2000, 478-pin available August 2001 1.6GHz: 423-pin available November 2000, 478-pin available August 2001 1.7GHz: 423-pin available November 2000, 478-pin available August 2001 1.8GHz: 423-pin available November 2000, 478-pin available August 2001 1.9GHz: 423-pin available November 2000, 478-pin available August 2001 2.0GHz: 423-pin available November 2000, 478-pin available August 2001
Chipset support	**Intel 850 with dual channel RDRAM memory** **Intel 845 with SDRAM memory**

[Desktop] Intel Pentium 4 Processor (Northwood)

Intel® Pentium® 4 for high performance desktop systems

Code name	**Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	*3.06GHz with 533MHz and all 800MHz system bus processors:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**400** or **533** or **800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Transistors	~55 million
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket**
Frequency and available date	1.6GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 2.0GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8A GHz with 400MHz system bus: available July 2002 2.0A GHz with 400MHz system bus: available January 2002 ("A" signifies the 0.13 micron version, not 0.18 micron) 2.2GHz with 400MHz system bus: available January 2002 2.26GHz with 533MHz system bus: available May 2002 2.4GHz with 400MHz system bus: available April 2002 2.4B GHz with 533MHz system bus: available May 2002 2.4C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.5GHz with 400MHz system bus: available August 2002 2.53GHz with 533MHz system bus: available May 2002 2.6GHz with 400MHz system bus: available August 2002 2.6C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.66GHz with 533MHz system bus: available August 2002 2.8GHz with 400MHz system bus: available April 2003 (used in ThinkPad G40) 2.8GHz with 533MHz system bus: available August 2002 2.8C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 3.0GHz with 800MHz system bus: available April 2003 with Hyper-Threading Technology 3.0GHz with 400MHz system bus: available April 2003 (used in ThinkPad G40) 3.06GHz with 533MHz system bus: available November 2002 with Hyper-Threading Technology 3.2GHz with 800MHz system bus: available June 2003 with Hyper-Threading Technology 3.4GHz with 800MHz system bus: available February 2004 with Hyper-Threading Technology
Chipset support	Intel 850 or 850E with dual channel RDRAM memory Intel 845 with SDRAM or DDR-SDRAM memory Intel 865 family with single or dual channel DDR-SDRAM memory (400, 533, or 800 MHz system bus) Intel 875P with single or dual channel DDR-SDRAM memory (800 MHz system bus)

[Desktop] Intel Pentium 4 Processor (Prescott)

Intel® Pentium® 4 for desktop systems

Code name	**Prescott**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	*800MHz system bus processors:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**533** or **800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Technology	90nm (nanometer) or 0.09u (micron)
Package and connector	**Flip-Chip Pin Grid Array (FC-mPGA4) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket**

Frequency and available date		
	2.80A GHz with 533MHz system bus	available February 2004
	2.80E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.00E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.20E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.40E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004

Chipset support	Intel 865 family with single or dual channel DDR-SDRAM memory Intel 875P with single or dual channel DDR-SDRAM memory

(34INTEL) Compiled by Roger Dodson, Lenovo. February 2004

[Desktop] Intel Pentium 4 Processor 5xx

Intel® Pentium® 4 for desktop systems	**Clock speed**	**L2 cache**	**System bus**	**Execute Disable Bit**	**Hyper-Threading Technology**	**Enhanced Intel SpeedStep™ Technology**	**Intel 64 Tech**	**Available date**
Intel Pentium 4 Processor 505	2.66GHz	1MB	533MHz	No	No	No	No	Jul 05
Intel Pentium 4 Processor 505J	2.66GHz	1MB	533MHz	**Yes**	No	No	No	Jul 05
Intel Pentium 4 Processor 506	2.66GHz	1MB	533MHz	**Yes**	No	No	**Yes**	Jul 05
Intel Pentium 4 Processor 515	2.93GHz	1MB	533MHz	No	No	No	No	Nov 04
Intel Pentium 4 Processor 516	2.93GHz	1MB	533MHz	No	No	No	**Yes**	Jun 05
Intel Pentium 4 Processor 519J	3.06GHz	1MB	533MHz	**Yes**	No	No	No	Jul 05
Intel Pentium 4 Processor 519 or 519K	3.06GHz	1MB	533MHz	**Yes**	No	No	**Yes**	Jul 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 520	2.8GHz	1MB	800MHz	No	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 520J	2.8GHz	1MB	800MHz	**Yes**	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 521	2.8GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 524	3.06GHz	1MB	533MHz	**Yes**	HT	No	**Yes**	July 06
Intel Pentium 4 Processor supporting Hyper-Threading Technology 530	3.0GHz	1MB	800MHz	No	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 530J	3.0GHz	1MB	800MHz	**Yes**	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 531	3.0GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 540	3.2GHz	1MB	800MHz	No	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 540J	3.2GHz	1MB	800MHz	**Yes**	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 541	3.2GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 550	3.4GHz	1MB	800MHz	No	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 550J	3.4GHz	1MB	800MHz	**Yes**	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 551	3.4GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 560	3.6GHz	1MB	800MHz	No	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 560J	3.6GHz	1MB	800MHz	**Yes**	HT	No	No	Jun 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 561	3.6GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05
Intel Pentium 4 Processor supporting Hyper-Threading Technology 570J	3.8GHz	1MB	800MHz	**Yes**	HT	No	No	Nov 04
Intel Pentium 4 Processor supporting Hyper-Threading Technology 571	3.8GHz	1MB	800MHz	**Yes**	HT	No	**Yes**	May 05

Code name	**Prescott**
Core	Single-core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	*Some:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable Bit	*Some:* protects memory data areas from malicious software execution
Intel 64 Technology[1]	*Some:* Intel 64 Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**533** or **800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Technology	90nm (nanometer) or 0.09u (micron)
Package and socket	**775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 915G, 915GV, 915P, 925X, and 925XE Express chipset or other compatible chipsets

Intel® Pentium® 4 supporting Hyper-Threading Technology for desktop systems

	Clock speed	L2 cache	Core	System bus	Intel Virtualization Technology	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Process	Available date
Intel Pentium 4 Processor 620	2.80GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	Aug 2006
Intel Pentium 4 Processor 630	3.00GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	Feb 2005
Intel Pentium 4 Processor 631	3.00GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	65nm	Jan 2006
Intel Pentium 4 Processor 640	3.20GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	Feb 2005
Intel Pentium 4 Processor 641	3.20GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	65nm	Jan 2006
Intel Pentium 4 Processor 650	3.40GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	Feb 2005
Intel Pentium 4 Processor 651	3.40GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	65nm	Jan 2006
Intel Pentium 4 Processor 660	3.60GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	Feb 2005
Intel Pentium 4 Processor 661	3.60GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	65nm	Jan 2006
Intel Pentium 4 Processor 662	3.60GHz	2MB	Single	800MHz	**Yes**	XD	HT	EIST	EM64T	90nm	Nov 2005
Intel Pentium 4 Processor 670	3.80GHz	2MB	Single	800MHz	No	XD	HT	EIST	EM64T	90nm	May 2005
Intel Pentium 4 Processor 672	3.80GHz	2MB	Single	800MHz	**Yes**	XD	HT	EIST	EM64T	90nm	Nov 2005

Code name	**Prescott** (90nm) or **Cedar Mill** (65nm)
Core	Single core
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ Technology
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology
Virtualization Technology	*Some:* Intel Virtualization Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**2MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Process technology	*Prescott:* 90nm (nanometer) or 0.09u (micron); *Cedar Mill:* 65nm (nanometer) or 0.065u (micron)
Package and socket	*6x0/6x2:* **775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T) *6x1:* **775-land Flip-Chip Land Grid Array (FC-LGA6) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 915 chipset family, 925X, 925XE, 945 chipset family, 955X, or other compatible chipsets

[Desktop] Intel Pentium D Processor 8xx

Intel® Pentium® Processor D Processor for desktop systems	**Clock speed**	**L2 cache**	**System bus**	**Package**	**Core**	**Hyper-Threading Technology**	**Total threads (logical)**	**Virtualization Technology**	**Execute Disable Bit**	**Enhanced Intel SpeedStep™ Technology**	**Intel 64 Tech**	**Available date**
Pentium D Processor 820	2.80GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	No	Yes	**No**	EM64T	Jun 05
Pentium D Processor 830	3.00GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	No	Yes	Yes	EM64T	Jun 05
Pentium D Processor 840	3.20GHz	2x1MB	800MHz	FC-LGA4	Dual	No	2	No	Yes	Yes	EM64T	Jun 05

Processor generation	Smithfield
Core	Dual-core
Formal name	**Intel Pentium D Processor**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	*Some:* Enhanced Intel SpeedStep™ Technology
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	No
L1 cache - bus	256-bit data path / full speed
L1 data cache	Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**Two 1MB** (one for each core) / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Technology (micron)	90nm or 0.09u
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 945 Express chipset family, 955X Express chipset

[Desktop] Intel Pentium D Processor 9xx

Intel® Pentium® Processor D Processor for desktop systems	Clock speed	L2 cache	System bus	Core	Hyper-Threading Technology	Total threads (logical)	Virtualization Technology	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Intel Viiv™ Tech	Available date
Pentium D Processor 915	2.80GHz	2x2MB	800MHz	Dual	No	2	**No**	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 920	2.80GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 925	3.00GHz	2x2MB	800MHz	Dual	No	2	**No**	Yes	Yes	EM64T	Viiv	Oct 06
Pentium D Processor 930	3.00GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 935	3.20GHz	2x2MB	800MHz	Dual	No	2	**No**	Yes	Yes	EM64T	Viiv	Jan 07
Pentium D Processor 940	3.20GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 945	3.40GHz	2x2MB	800MHz	Dual	No	2	**No**	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 950	3.40GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	Jan 06
Pentium D Processor 960	3.60GHz	2x2MB	800MHz	Dual	No	2	Yes	Yes	Yes	EM64T	Viiv	May 06

Processor generation	Presler
Core	Dual-core
Formal name	**Intel Pentium D Processor**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ Technology
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	*Some:* Intel Virtualization Technology
Viiv Technology	Intel Viiv Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**Two 2MB** (one for each core) / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Process technology	65nm or 0.065u
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 945 Express chipset family, 955X and 975X Express chipset

[Desktop] Intel Pentium 4 Processor Extreme Edition

Intel® Pentium® 4 Processor Extreme Edition for high-end gamers and power users	Clock speed	L2 cache	L3 cache	System bus	Core	Package	Execute Disable Bit	Hyper-Threading Technology	Enhanced Intel SpeedStep™ Technology	EM64T	Available date
Intel Pentium 4 Processor Extreme Edition	3.2GHz	512KB	2MB	800MHz	Single	FC-PGA2	No	HT	No	No	Nov 03
Intel Pentium 4 Processor Extreme Edition	3.4GHz	512KB	2MB	800MHz	Single	FC-PGA2	No	HT	No	No	Feb 04
Intel Pentium 4 Processor Extreme Edition	3.4GHz	512KB	2MB	800MHz	Single	FC-LGA4	No	HT	No	No	Jun 04
Intel Pentium 4 Processor Extreme Edition	3.46GHz	512KB	2MB	1066MHz	Single	FC-LGA4	No	HT	No	No	Nov 04
Intel Pentium 4 Processor Extreme Edition	3.73GHz	2MB	None	1066MHz	Single	FC-LGA4	Yes	HT	No	Yes	Feb 05

Code name	None (3.73GHz is Prescott)
Core	Single core
Formal name	**Intel Pentium 4 Processor with HT Technology Extreme Edition**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	*3.73GHz only:* Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	None
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Execute Disable (XD) Bit	*3.73GHz only:* protects memory data areas from malicious software execution
EM64T	*3.73GHz only:* Extended Memory 64 Technology

L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** or **2MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	*Some:* None *Some:* **2MB** / full speed / 256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / parity / integrated / unified (internal die; on die)
System bus	**800MHz** or **1066MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software (some compatible with EM64T software)
Multiple processors	No SMP support
Technology (micron)	0.13u (3.73GHz is 90nm or 0.09u)
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket** or **775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 848P, 865 family, and 875P for FC-PGA2 package Intel 915G, 915P, 925X, and 925XE Express chipset for FC-LGA4 package Intel 925XE Express supports 1066MHz system bus

Mobile Intel Pentium 4 Processor 5xx

Mobile Intel® Pentium® 4 processor for mobile systems

	Clock speed	L2 cache	Execute Disable Bit	System bus	Hyper-Threading Technology	Available date
Mobile Intel Pentium 4 Processor 518	2.8GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 532	3.06GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 538	3.2GHz	1MB	No	533MHz	Hyper-Threading Technology	June 2004
Mobile Intel Pentium 4 Processor 548	3.33GHz	1MB	No	533MHz	Hyper-Threading Technology	September 2004
Mobile Intel Pentium 4 Processor 552	3.46GHz	1MB	No	533MHz	Hyper-Threading Technology	January 2005

Messaging	Second generation Mobile Intel Pentium 4 processor designed for larger-sized notebooks also known as "desktop replacements" typically featuring large screens, full-size keyboards, and multiple drives
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
Execute Disable Bit	No

L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)

L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None

System bus	**533MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 266MHz
System bus - width	64-bit data path

Execution units	2 integer units; 1 floating point unit; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers

Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan

Process technology	90nm (nanometer) or 0.09u (micron)
Package and connector	**Flip-Chip Pin Grid Array (FC-mPGA4) package** **requires 478-pin surface mount Zero Insertion Force (ZIF) socket (mPGA478B socket)**

		Performance Mode	*Battery Mode*
Frequency	**2.8GHz**	**2.8GHz, 88 watts at 1.25-1.40 volts**	**1.86GHz, 1.15 volts**
	3.06GHz	**3.06GHz, 88 watts at 1.25-1.40 volts**	**1.86GHz, 1.15 volts**
	3.2GHz	**3.2GHz, 88 watts at 1.25-1.40 volts**	**1.86GHz, 1.15 volts**
	3.33GHz	**3.33GHz, 88 watts at 1.25-1.40 volts**	**1.86GHz, 1.15 volts**
	3.46GHz	**3.46GHz, 88 watts at 1.25-1.40 volts**	**1.86GHz, 1.15 volts**

Chipset support	**Intel 852GME, 852PM chipsets** **Other compatible chipsets**

[Desktop] Intel Pentium Processor Extreme Edition 8xx

Intel® Pentium® Processor Extreme Edition for high-end gamers and power users	**Clock speed**	**L2 cache**	**System bus**	**Package**	**Core**	**Hyper-Threading Technology**	**Total threads (logical)**	**Execute Disable Bit**	**Enhanced Intel SpeedStep™ Technology**	**Intel 64 Tech**	**Available date**
Pentium Processor Extreme Edition 840	3.20GHz	2x1MB	800MHz	FC-LGA4	Dual	Yes	4	Yes	No	EM64T	Apr 05

Processor generation	Smithfield
Core	Daul core
Formal name	**Intel Pentium Processor Extreme Edition**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	None
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Total threads	Four threads (two cores each supporting Hyper-Threading provides four logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
L1 cache - bus	256-bit data path / full speed
L1 data cache	Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**Two 1MB** (one for each core) / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Technology (micron)	90nm or 0.09u
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA4) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 955X Express chipset

[Desktop] Intel Pentium Processor Extreme Edition 9xx

Intel® Pentium® Processor Extreme Edition for high-end gamers and power users	**Clock speed**	**L2 cache**	**System bus MHz**	**Package**	**Core**	**Hyper-Threading Technology**	**Total threads (logical)**	**Virtual-ization Tech**	**Execute Disable Bit**	**Enhanced Intel SpeedStep™ Technology**	**Intel 64 Tech**	**Available date**
Pentium Processor Extreme Edition 955	3.46GHz	2x2MB	1066	FC-LGA6	Dual	Yes	4	Yes	Yes	No	EM64T	Jan 06
Pentium Processor Extreme Edition 965	3.73GHz	2x2MB	1066	FC-LGA6	Dual	Yes	4	Yes	Yes	No	EM64T	Mar 06

Processor generation	Presler
Core	Dual-core
Formal name	**Intel Pentium Processor Extreme Edition**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	None
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Total threads	Four threads (two cores each supporting Hyper-Threading provides four logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	Intel 64 Technology (an extension to the IA-32 instruction set which adds 64 bit extensions to the x86 architecture)
Virtualization Technology	Intel Virtualization Technology
L1 cache - bus	256-bit data path / full speed
L1 data cache	Two 16KB data caches / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / two instruction caches (each hold 12,000 micro-ops) / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**Two 2MB** (one for each core) / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**1066MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 and EM64T software
Process technology	65nm or 0.065u
Package and connector	**775-land Flip-Chip Land Grid Array (FC-LGA6) package requires LGA775 socket** (socket also called Socket T)
Chipset support	Intel 975X Express chipset

Intel Core Solo Processor

Intel® Core™ Solo processor for mobile and desktop systems	Clock Perf Mode	Clock Battery Mode	L2 cache	System bus MHz	Core	Hyper-Threading Technology	Total threads (logical)	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail-able date
Ultra Low Voltage (ULV)												
Intel Core Solo processor ULV U1300	1.06GHz	800MHz	2MB	533MHz	Single	No	1	Yes	Yes	Yes	No	Apr 2006
Intel Core Solo processor ULV U1400	1.20GHz	800MHz	2MB	533MHz	Single	No	1	Yes	Yes	Yes	No	Apr 2006
Intel Core Solo processor ULV U1500	1.33GHz	800MHz	2MB	533MHz	Single	No	1	Yes	Yes	Yes	No	Jan 2007
Intel Core Solo processor T1300	1.66GHz	1.0GHz	2MB	667MHz	Single	No	1	No	Yes	Yes	No	Jan 2006
Intel Core Solo processor T1400	1.83GHz	1.0GHz	2MB	667MHz	Single	No	1	No	Yes	Yes	No	May 2006

U=<14 watts; L=15-24 watts; T=25-49 watts; E=>50 watts

Processor generation	**Yonah**
Marketing name	**Intel Core Solo processor**
Core	**Single-core**
Branding	Part of the **Intel Centrino™ mobile technology** when included with an Intel 945 Express Chipset family and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, Advanced Stack Management
MMX™ / Streaming SIMD	MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Dynamic Bus Parking, Enhanced Deeper Sleep with Dynamic Cache Sizing
Thermal management	Thermal management system (digital temperature sensor and thermal monitor)
Hyper-Threading	No
Total threads	One thread (one core with no Hyper-Threading support provides one logical processor)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	No
Virtualization Technology	*Some:* Intel Virtualization Technology
L1 cache - bus	256-bit data path, full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**2MB** / full speed / Advanced Transfer Cache
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	**533** or **667MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 333MHz
System bus - width	64-bit data path
Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Power	*U1xxx:* 5.0-5.5 watts; *T1300:* 27 watts
Package and connector	Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball) [Ultra Low Voltage offered only in Micro Flip-Chip Ball Grid Array (Micro-FCBGA)]
Chipset support	**Intel 945 Express Chipset family**, other compatible chipsets

(C1INTEL) Compiled by Roger Dodson, Lenovo. December 2008

Intel Core Duo Processor

Intel® Core™ Duo processor for mobile and desktop systems	Clock Perf Mode	Clock Battery Mode	Shared L2 cache	System bus MHz	Core	Hyper-Threading Technology	Total threads (logical)	Virtual-ization Tech	Execute Disable Bit	Enhanced Intel SpeedStep™ Technology	Intel 64 Tech	Avail-able date
Intel Core Duo processor U2400	1.06GHz	800MHz	2MB	533MHz	Dual	No	2	Yes	Yes	Yes	No	Sep 2006
Intel Core Duo processor U2500	1.20GHz	800MHz	2MB	533MHz	Dual	No	2	Yes	Yes	Yes	No	Jun 2006
Intel Core Duo processor L2300	1.50GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor L2400	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor L2500	1.83GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Sep 2006
Intel Core Duo processor T2300	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2300E	1.66GHz	1.0GHz	2MB	667MHz	Dual	No	2	**No**	Yes	Yes	No	May 2006
Intel Core Duo processor T2350	1.86GHz	800MHz	2MB	533MHz	Dual	No	2	**No**	Yes	Yes	No	Jan 2007
Intel Core Duo processor T2400	1.83GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2450	2.00GHz	800MHz	2MB	533MHz	Dual	No	2	**No**	Yes	Yes	No	Jun 2007
Intel Core Duo processor T2500	2.00GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2600	2.16GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jan 2006
Intel Core Duo processor T2700	2.33GHz	1.0GHz	2MB	667MHz	Dual	No	2	Yes	Yes	Yes	No	Jun 2006

U (Ultra Low Voltage)=<14 watts; L (Low Voltage)=15-24 watts; T (Standard Voltage)=25-49 watts; E=>50 watts

Processor generation	**Yonah**
Marketing name	**Intel Core Duo processor**
Core	**Dual-core**
Branding	Part of the **Intel Centrino™ Duo mobile technology** when included with an Intel 945 Express Chipset family and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, Advanced Stack Management
MMX™ / Streaming SIMD	MMX™ (57 new instructions), Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Dynamic Bus Parking, Enhanced Deeper Sleep with Dynamic Cache Sizing
Thermal management	Thermal management system (digital temperature sensor and thermal monitor on each core)
Hyper-Threading	No
Total threads	Two threads (two cores with no Hyper-Threading support provide two logical processors)
Execute Disable (XD) Bit	Protects memory data areas from malicious software execution
Intel 64 Technology[1]	No
Virtualization Technology	*Some:* Intel Virtualization Technology
L1 cache - bus	256-bit data path, full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**2MB** / full speed / shared between both cores (Smart Cache) / Advanced Transfer Cache / Data Cache Unit Streamer
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (on die)
L3 cache	None
System bus	**533** or **667MHz** (transfers data 4 times per clock) / address bus transfers at 2 times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 333MHz
System bus - width	64-bit data path
Execution units	2 integer units, 1 floating point units, 1 load unit, 1 store unit
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Process technology	65nm or 0.065u
Power	*U2xxx:* 9 watts; *L2xxx:* 15 watts; *T2xxx:* 31 watts
Package and connector	Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)
Chipset support	**Mobile Intel 945 Express Chipset family**, other compatible chipsets

PC Processors (Xeon - Foster)

Intel® Xeon™ processor for high-performance and mid-range, dual processor enabled workstations

Code name	**Foster**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache	**None**
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	**2-way SMP support**
Systems management	Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron)	0.18u
Transistors	~42 million
Package type	**603-pin micro-Pin Grid Array (PGA)**
Connector	**Zero Insertion Force (ZIF) socket with 603 pins**
Frequency (MHz) and available date	1.4GHz with 400MHz FSB (available May 2001) 1.5GHz with 400MHz FSB (available May 2001) 1.7GHz with 400MHz FSB (available May 2001) 2.0GHz with 400MHz FSB (available September 2001)
Chipset support	**Intel 860 with dual channel RDRAM memory**

PC Processors (Xeon - Prestonia)

Intel® Xeon™ processor for high-performance and mid-range, dual processor enabled workstations

Code name	**Prestonia**
Positioning	**Dual-processing (DP) workstations**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	**Hyper-Threading (HT) Technology** (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache	**None**
System bus	**400 or 533MHz** (transfers data four times per clock [100MHz x 4 = 400MHz or 133MHz x 4 = 533MHz]) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at two times clock [100MHz x 2 = 200MHz or 133MHz x 2 = 266MHz]
System bus - width	64-bit data path
Execution units	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	**2-way SMP support**
Systems management	*400MHz:* thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus *533MHz:* supports direct access to pins of on-die thermal diode for thermal sensor device
Technology (micron)	0.13u
Package type	*400MHz:* **603-pin interposer micro-Pin Grid Array (INT-mPGA)** *500MHz:* **604-pin flip-chip micro-PGA2 (FC-mPGA2)**
Connector	**Zero Insertion Force (ZIF) socket with 603 or 604 pins**
Frequency (GHz) and available date	1.8GHz with 400MHz system bus (available February 2002) 2.0GHz with 400MHz system bus (available February 2002) 2.0GHz with 533MHz system bus (available November 2002) 2.2GHz with 400MHz system bus (available February 2002) 2.4GHz with 400MHz system bus (available April 2002) 2.4GHz with 533MHz system bus (available November 2002) 2.6GHz with 400MHz system bus (available September 2002) 2.66GHz with 533MHz system bus (available November 2002) 2.8GHz with 400MHz system bus (available September 2002) 2.8GHz with 533MHz system bus (available November 2002) 3.0GHz with 533MHz system bus (available March 2003) 3.06GHz with 533MHz system bus (available March 2003)
Chipset support	**Intel 860 with dual channel RDRAM memory** **Intel E750x (such as E7500, E7501, E7505) with dual channel DDR-SDRAM** **ServerWorks® Grand Champion™ 4.0 LE**
Server blade support	Most Xeon processors listed above supported in "Performance Server Blades"

PC Processors (Xeon MP)

Intel® Xeon™ Processor MP for mid-tier and back-end servers with 4-way SMP support

Code name	**Foster MP**
Positioning	**Multi-processing (MP) workstations and servers**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	**Hyper-Threading (HT) Technology** (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache	**512KB** or **1MB** / full speed
L3 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / parity / integrated / unified (internal die; on die)
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	**4-way SMP support**
Systems management	Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron)	0.18u
Package type	**603-pin interposer micro-Pin Grid Array (INT-mPGA)**
Connector	**Zero Insertion Force (ZIF) socket with 603 pins**
Frequency (GHz) and available date	1.4GHz with 512KB L3 cache (available March 2002) 1.5GHz with 512KB L3 cache (available March 2002) 1.6GHz with 1MB L3 cache (available March 2002)
Chipset support	**IBM® XA-32™** **ServerWorks® GC-HE**
Server blade support	Xeon MP at 1.6GHz supported in "Performance Server Blades"

(25INTEL) Compiled by Roger Dodson, IBM. March 2002

PC Processors (Xeon MP - Gallatin)

Intel® Xeon™ Processor MP for mid-tier and back-end servers with 4-way or more SMP support

Code name	**Gallatin**
Positioning	**Multi-processing (MP) workstations and servers (4-way or more SMP)**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	**Hyper-Threading Technology** (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / ECC / integrated / unified (internal die; on die)
L3 cache	**1MB** or **2MB** / full speed
L3 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / ECC / integrated / unified (internal die; on die)
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	3 integer units; 2 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	**4-way or more SMP support**
Systems management	Thermal monitor, Processor Information ROM (PIROM), OEM Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron)	0.13u
Package type	**603-pin interposer micro-Pin Grid Array (INT-mPGA)**
Connector	**Zero Insertion Force (ZIF) socket with 603 pins**
Frequency (GHz) and available date	1.5GHz with 1MB L3 cache (available November 2002) 1.9GHz with 1MB L3 cache (available November 2002) 2.0GHz with 2MB L3 cache (available November 2002)
Chipset support	**IBM® XA-32™** **ServerWorks® GC-HE**

(31INTEL) Compiled by Roger Dodson, IBM. November 2002

Intel® Itanium® for 64-bit demanding enterprise and computing applications

	733MHz, 800MHz
Code name	**Merced**
Architecture	IA-64 (Intel Architecture 64-bit) / Explicitly Parallel Instruction Set Computing (EPIC)
MMX™ / SIMD	IA-64 multimedia instructions are semantically compatible with MMX and Streaming SIMD Extensions instructions
L1 cache	**32KB** L1 cache (16KB instruction cache and 16KB data cache) / integrated in die / full speed / 4-way set associative / 32 byte cache line / unpublished data path / parity protected / 2 cycle latency
L2 cache	**96KB** L2 cache (unified) / integrated in die / full speed / 6-way set associative 64 byte cache line / 256-bit data path (32 bytes) / L2 tag parity protected / L2 data is ECC protected / 6 cycle latency (with the 2 cycle L1 miss) / 9 cycle latency for floating point loads
L3 cache	**2MB or 4MB** L3 cache (unified) / off die, on cartridge / full speed / 4-way set associative / 64 byte cache line / 128-bit data path (16 bytes) / L2 tag and data is ECC protected / 21 cycle latency / 24 cycle latency for floating point loads
Front Side Bus	**266MHz** (double pumped 133MHz bus) / 64-bit data path / ECC / cache line size is chipset dependent
Memory addressability	44-bit address bus for 18TB memory addressability / 256MB maximum page size / Merced limited to 36-bit addressability or 64GB (460GX also limits to 64GB) / compatible with flat 64-bit address model with 18EX (18 exabytes) memory addressability, but chipset dependent
Execution units	2 integer units, 2 memory units, 2 floating point units, 3 branch exection units / able to execute 4 ALU instructions per clock / 2 loads or stores per clock / 9 issue ports
Floating point	Each floating point unit contains a Floating Point Multiply Accumulate (FMAC) that operates on 82-bit operands / each FMAC unit can execute two floating point operations per clock with single, double and double-extended precision
Registers	128 integer registers, 128 floating point registers, 8 branch registers, 64 1-bit predicate registers
Out-of-order instructions	No / 10 stage in-order pipeline
EPIC features	Predication: speculatively executes instructions along both branch paths and then discards the results not needed Speculation: speculatively loads data before needed and still tries to find the data in the caches first Compiler: reorders and optimizes instruction stream at compile time Bundle: uses three 41-bit instructions and an 5-bit template into a 128-bit fixed length bundle Register stacking: reduces call/return procedure overhead via the flexible integer register model managed by the Register Stack Engine (RSE) Register rotation: automatically renames registers in hardware to improve software loop performance
Compatibility	Native IA-64 support / IA-32 instruction compatibility in hardware
Multiple processors	Initial version supports up to 4-way SMP support
Systems management	Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron)	0.18u
Transistors	~25 million in die (core) / ~300 million in die and L3 cache
Package type	**418-pin array cartridge (418PAC)**
Connector	**Requires 418-pin Low Insertion Force (LIF) Socket M and one Power Pod per processor**
Frequency (MHz) and available date	733MHz with 2MB L3 cache (available July 2001) 733MHz with 4MB L3 cache (available July 2001) 800MHz with 2MB L3 cache (available July 2001) 800MHz with 4MB L3 cache (available July 2001)
Chipset support	**Intel 460GX with SDRAM PC100 memory (limits to 36-bit addressing to 64GB memory addressability))**

(15INTEL) Compiled by Roger Dodson, IBM. June 2001

Intel® Itanium® 2 for 64-bit demanding enterprise and computing applications

Code name	**McKinley**
Architecture	IA-64 (Intel Architecture 64-bit) / Explicitly Parallel Instruction Set Computing (EPIC) / Intel Itanium architecture
MMX™ / SIMD	IA-64 multimedia instructions are semantically compatible with MMX and Streaming SIMD Extensions instructions
L1 cache	**32KB** L1 cache (16KB instruction cache and 16KB data cache) / integrated in die / full speed / 4-way set associative / write-through data cache / 64 byte cache line / unpublished data path / parity protected / 1 cycle latency
L2 cache	**256KB** L2 cache (unified) / integrated in die / full speed / 8-way set associative / write-back / 128 byte cache line / 256-bit data path (32 bytes) / L2 data and L2 tag is ECC protected / 5 cycle latency / 6 cycle latency for floating point loads
L3 cache	**1.5MB or 3MB** L3 cache (unified) / integrated in die / full speed / 12-way set associative / write-back / 128 byte cache line / 128-bit data path (16 bytes) / L3 tag and data is ECC protected / 12 cycle latency
System bus	**400MHz** (quad pumped 100MHz bus) / 128-bit data path / 6.4GB/sec throughput / ECC / cache line size is chipset dependent
Memory addressability	50-bit address bus for 1PB memory addressability / 4GB maximum page size / compatible with flat 64-bit address model with 18EX (18 exabytes) memory addressability, but chipset dependent
Execution units	4 memory/ALU/multimedia units, 2 integer/ALU/multimedia units, 2 load units, 2 store units, 3 branch units, 2 extended-precision floating point units, 1 single-precision floating point unit / able to execute 6 instructions per clock / 2 loads and stores per clock / 11 issues ports
Registers	128 integer registers, 128 floating point registers, 8 branch registers, 64 1-bit predicate registers
Out-of-order instructions	No / 8 stage in-order pipeline
EPIC features	Predication: speculatively executes instructions along both branch paths and then discards the results not needed Speculation: speculatively loads data before needed and still tries to find the data in the caches first Compiler: reorders and optimizes instruction stream at compile time Bundle: uses three 41-bit instructions and an 5-bit template into a 128-bit fixed length bundle Register stacking: reduces call/return procedure overhead via the flexible integer register model managed by the Register Stack Engine (RSE) Register rotation: automatically renames registers in hardware to improve software loop performance
Compatibility	Native IA-64 support / IA-32 instruction compatibility in hardware
Multiple processors	Natively supports up to 8-way SMP support / enabled for >8-way SMP
Systems management	Thermal sensor, Processor Information EEPROM (PIROM), Scratch EEPROM, Systems Management Bus (SMBus)
Technology (micron)	0.18u
Package type	**611-pin array cartridge (PAC611)**
Connector	**Requires mPGA700 Zero Insertion Force (ZIF) Socket and one Power Pod per processor**
Frequency (MHz) and available date	900MHz with 1.5MB L3 cache (available July 2002) 1GHz with 1.5MB L3 cache (available July 2002) 1GHz with 3MB L3 cache (available July 2002)
Chipset support	**Intel E8870 chipset, OEM custom chipset, IBM XA-64™ chipset**

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[1] **Intel 64 Technology (formerly EM64T):** Intel 64 Technology (formerly Intel EM64T) requires a computer system with a processor, chipset, BIOS, operating system, device drivers, and applications enabled for Intel 64 Technology. Processor will not operate (including 32-bit operation) without an Intel 64 Technology-enabled BIOS. Performance will vary depending on your hardware and software configurations.

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